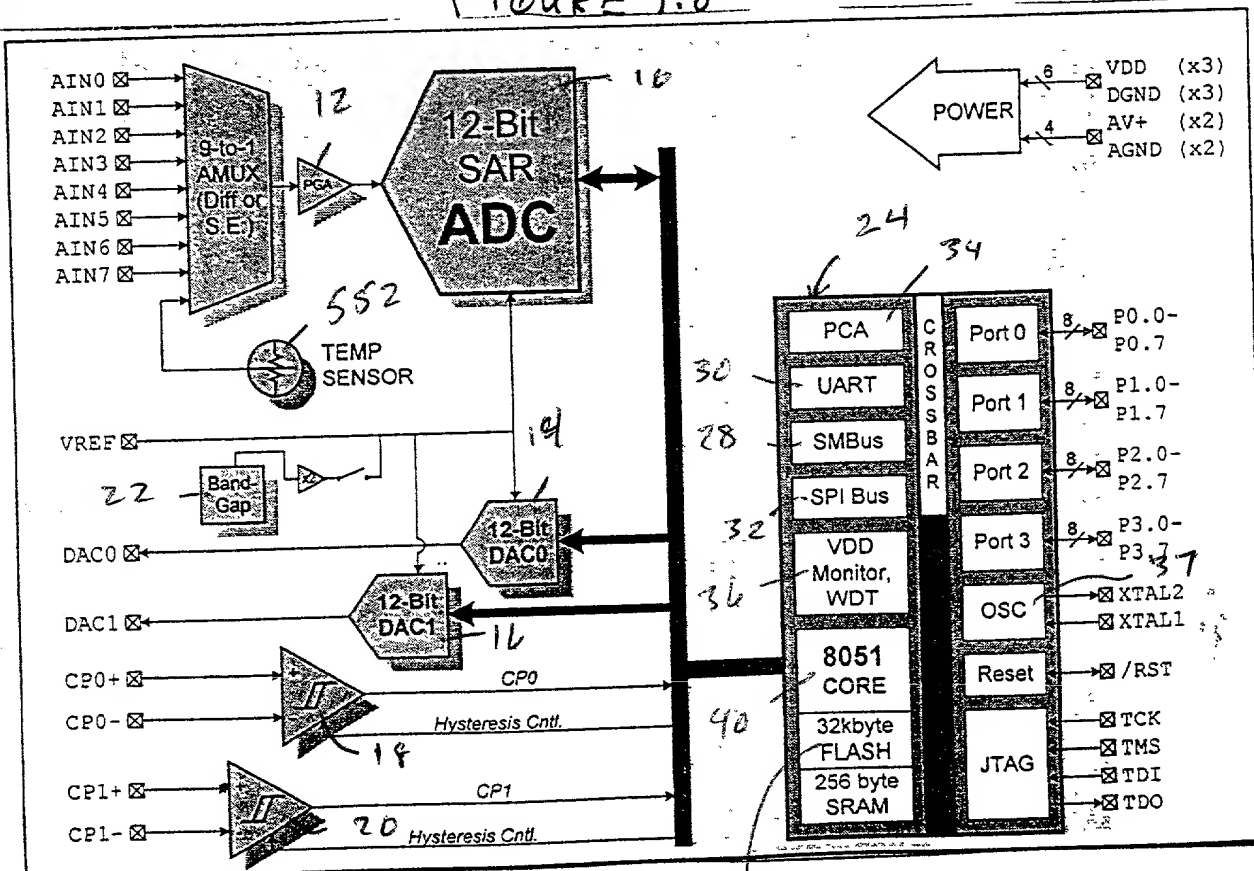


FIGURE 1.0

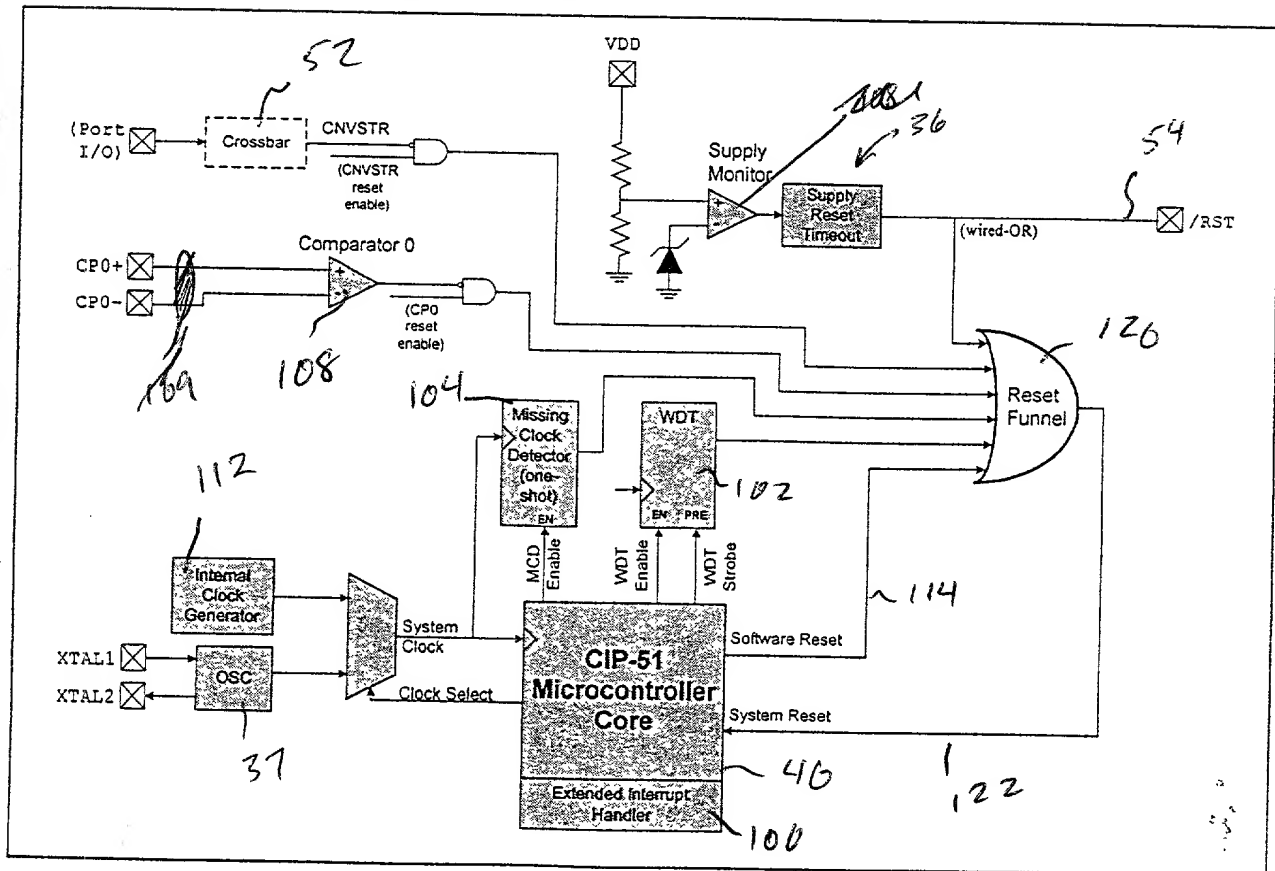
1061500 5158660





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### Figure 1.3. On-Board Clock and Reset



4  
4  
Figure 1.4. On-Board Memory Map

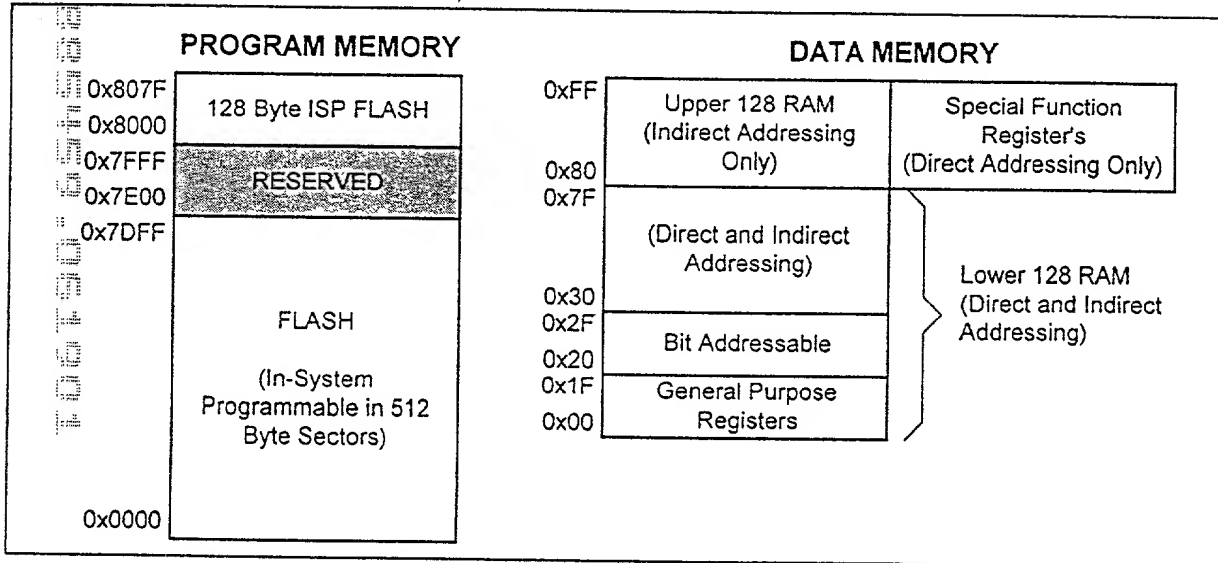


Figure 1/5. Emulation Diagram

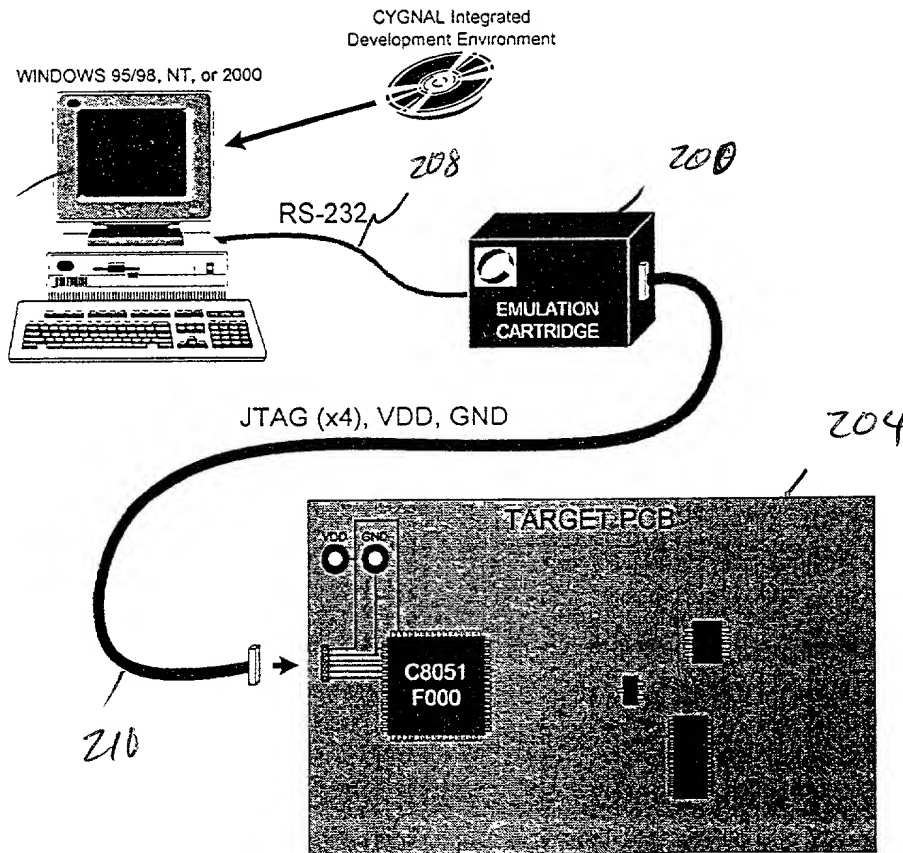
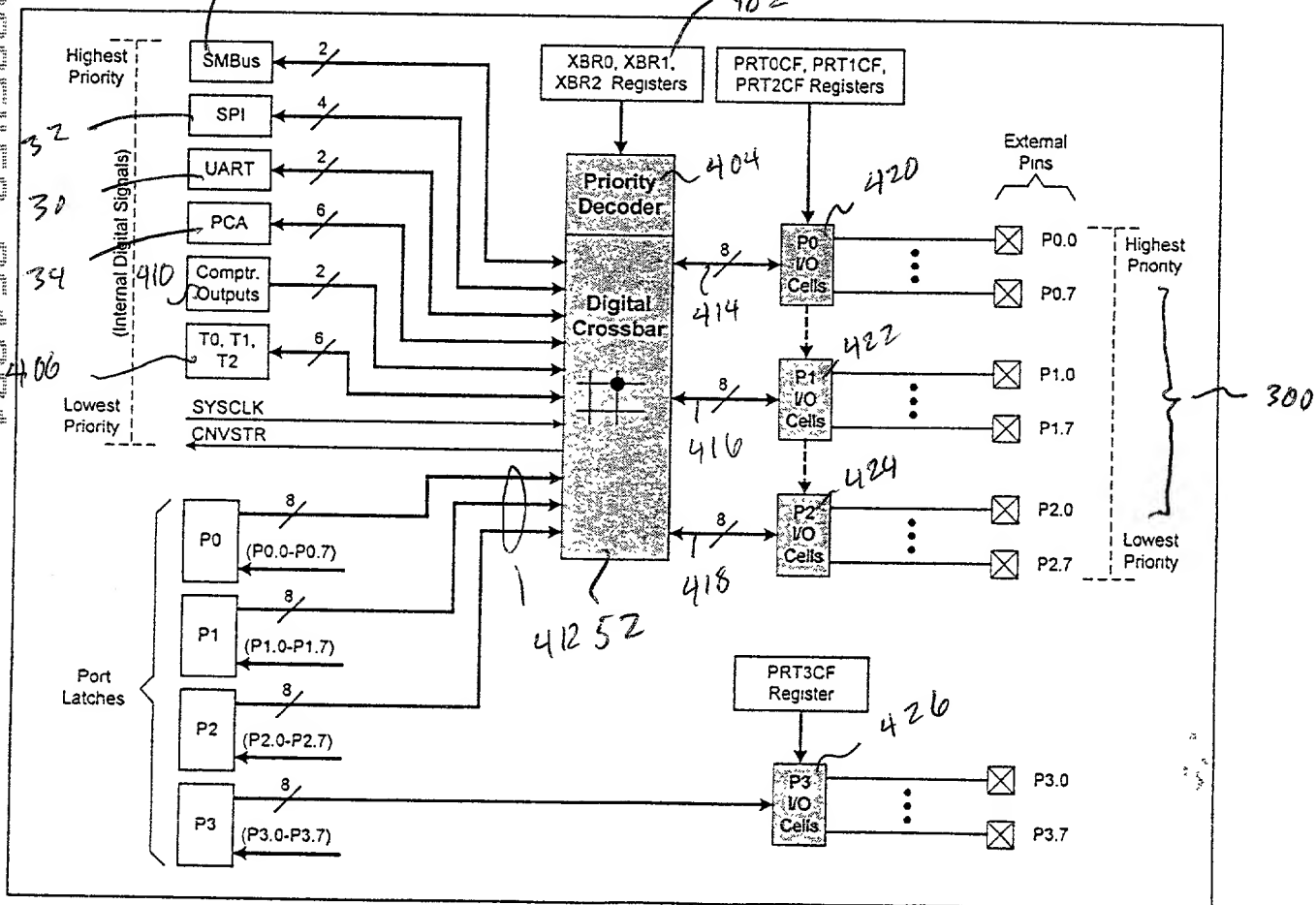
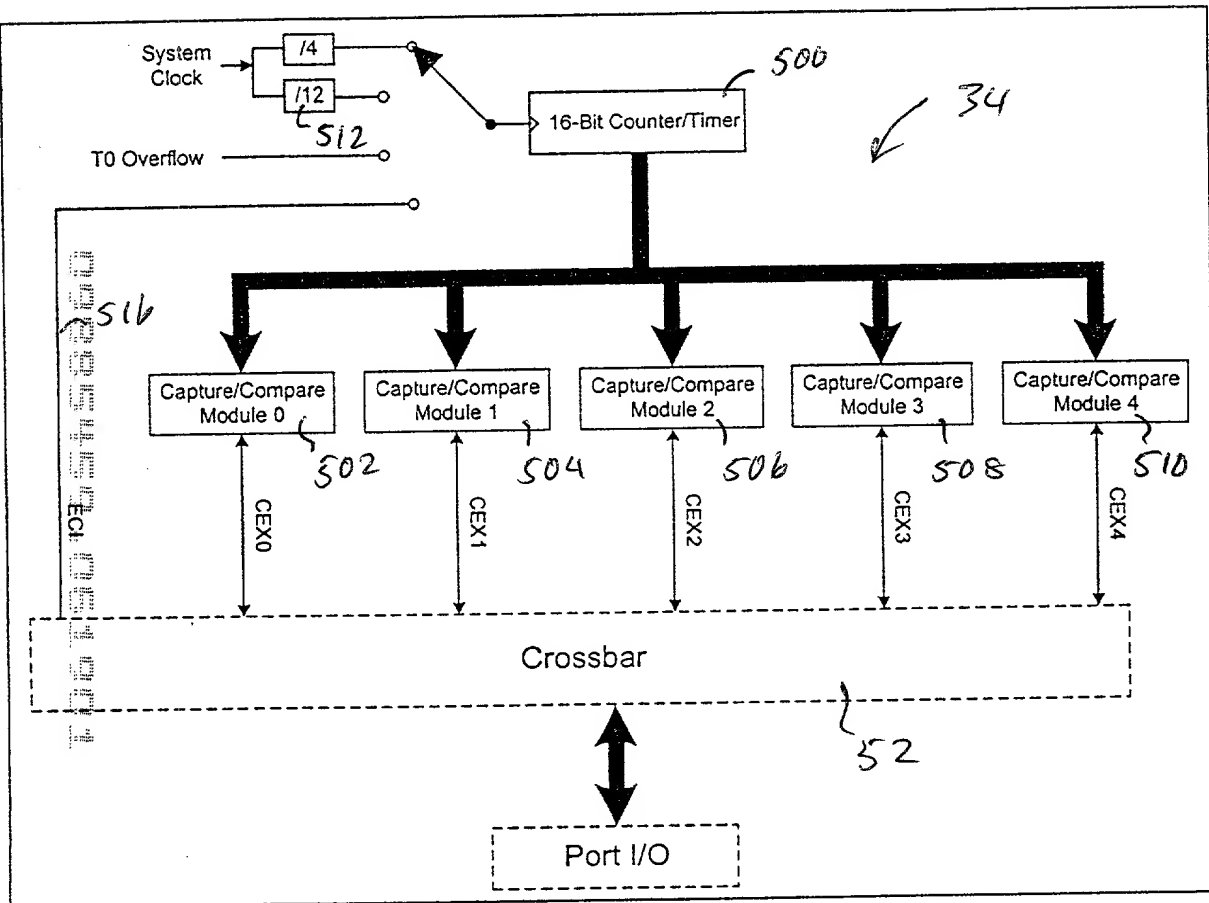


Figure 1.6. Digital Crossbar Diagram

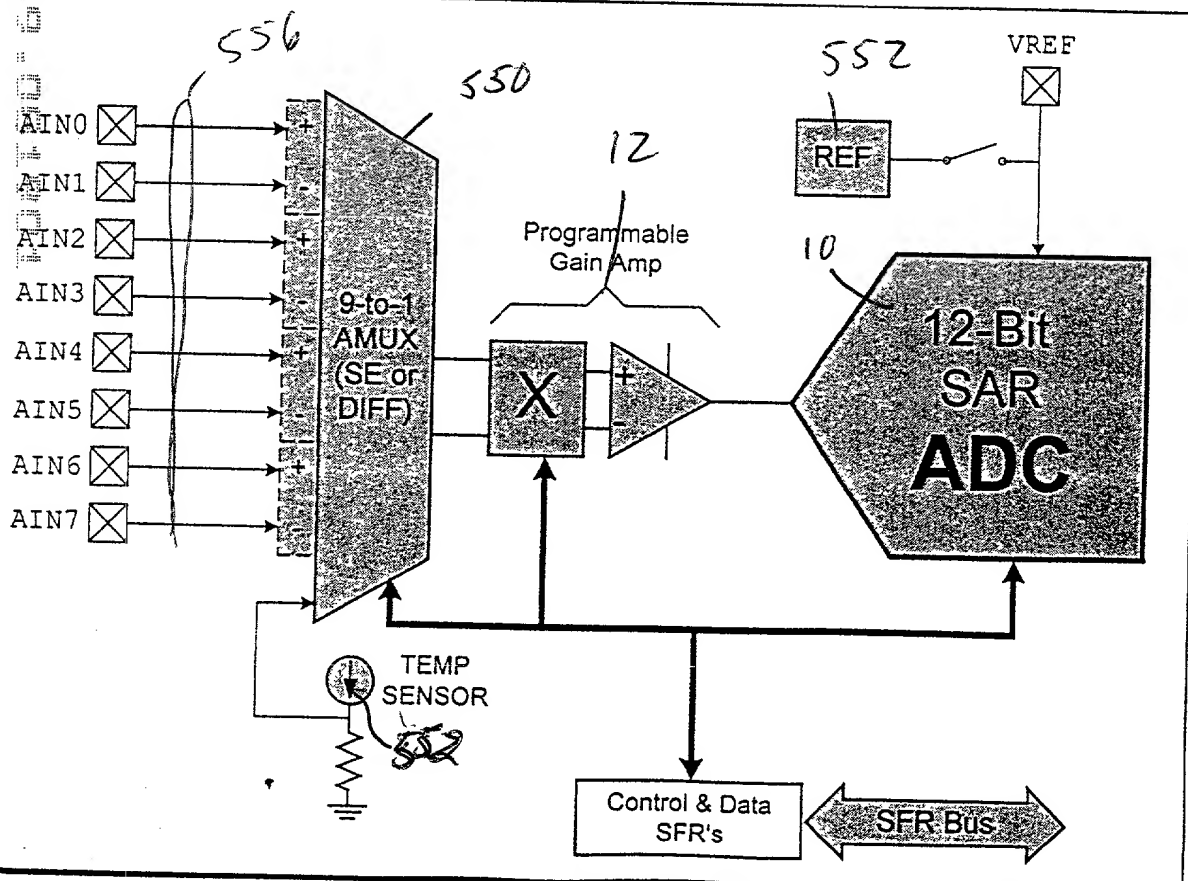


87  
Figure 1.7. PCA Block Diagram



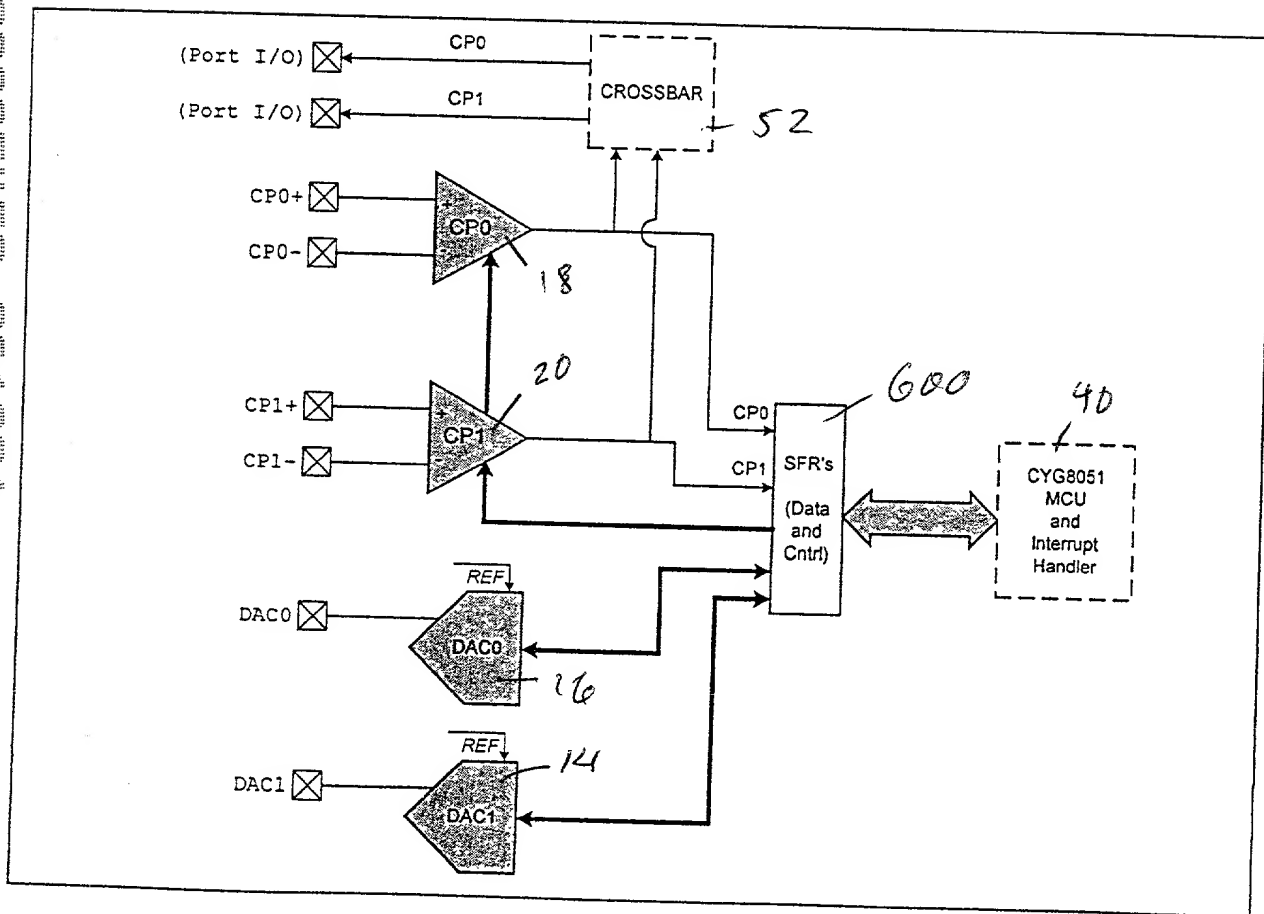
A008

Figure 1.8. ADC Diagram



9  
~~18~~

Figure 1.9. Comparator and DAC Diagram



**Figure 5.1. ADC Functional Block Diagram**

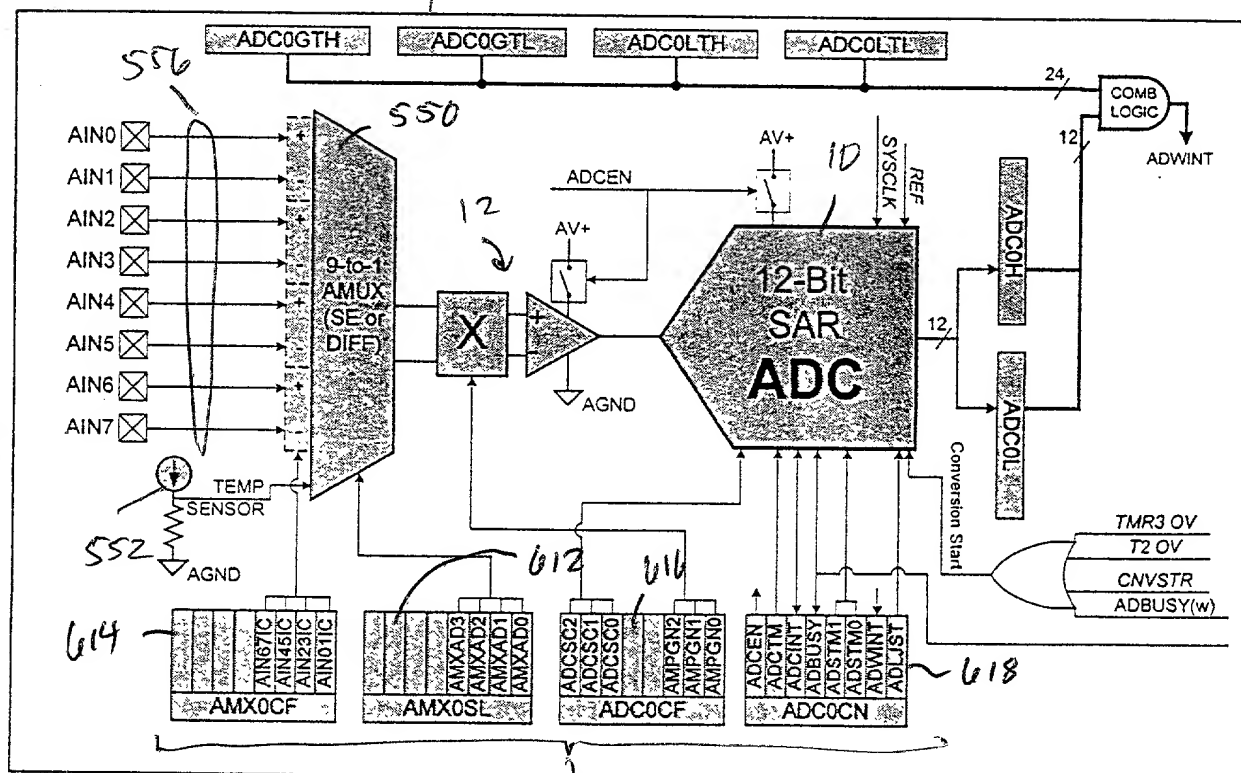
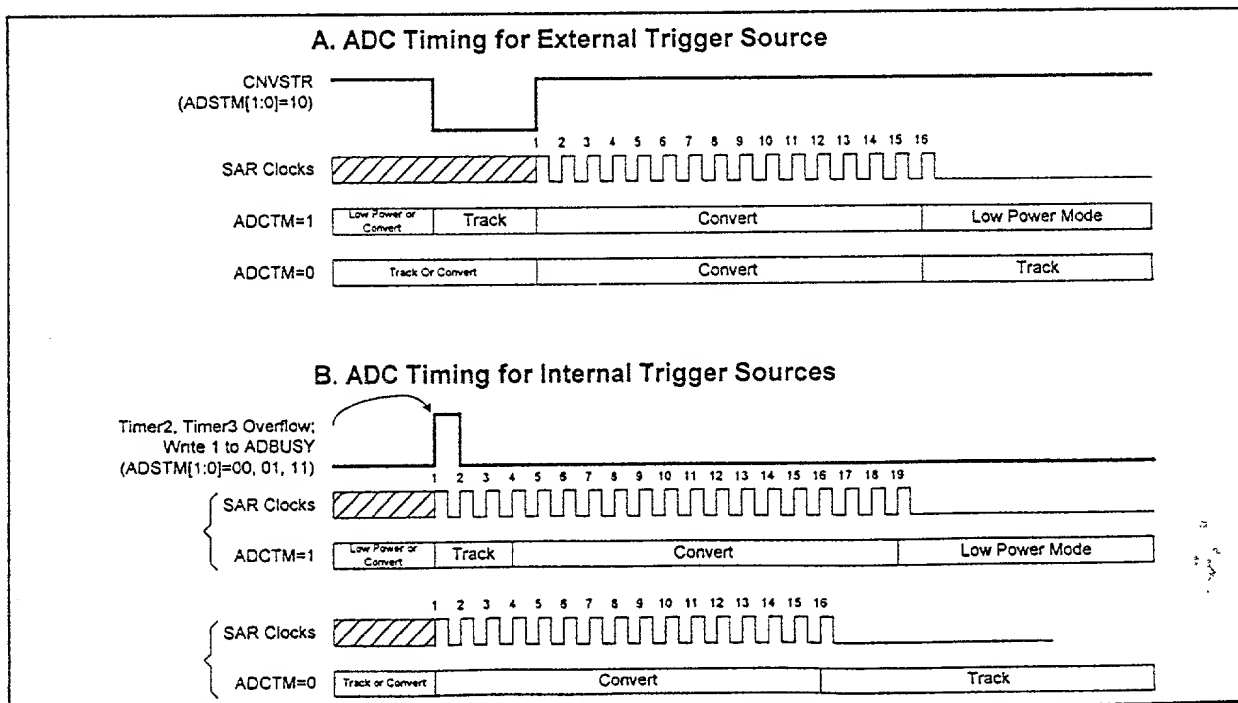


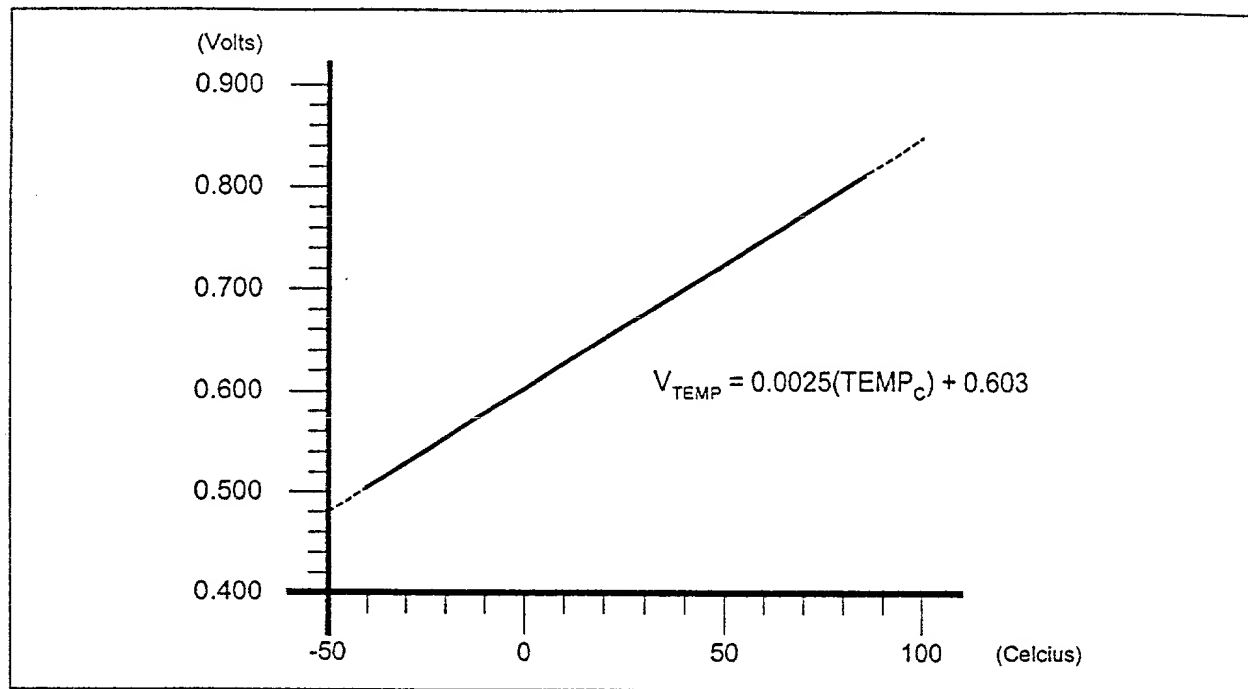
Figure 5.2. ADC Track and Conversion Example Timing



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12  
48

Figure 5.3. Temperature Sensor Transfer Function



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Figure 5.14: ADC Window Interrupt Examples, Right Justified Data

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0x0FFF	ADWINT not affected
	0x0201	
REF x (512/4096)	0x0200	ADC0LTH:ADC0LTL
	0x01FF	ADWINT=1
	0x0101	
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL
	0x00FF	ADWINT not affected
0	0x0000	

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,  
 ADC0LTH:ADC0LTL = 0x0200,  
 ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0200 and > 0x0100.

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0x0FFF	ADWINT=1
	0x0201	
REF x (512/4096)	0x0200	ADC0GTH:ADC0GTL
	0x01FF	ADWINT not affected
	0x0101	
REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	ADWINT=1
0	0x0000	

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,  
 ADC0LTH:ADC0LTL = 0x0100,  
 ADC0GTH:ADC0GTL = 0x0200.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 or > 0x0200.

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x07FF	ADWINT not affected
	0x0101	
REF x (256/4096)	0x0100	ADC0LTH:ADC0LTL
	0x00FF	ADWINT=1
	0x0000	
REF x (-1/4096)	0xFFFF	ADC0GTH:ADC0GTL
	0xFFFE	ADWINT not affected
-REF	0xF800	

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0,  
 ADC0LTH:ADC0LTL = 0x0100,  
 ADC0GTH:ADC0GTL = 0xFFFF.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 and > 0xFFFF. (Two's

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x07FF	ADWINT=1
	0x0101	
REF x (256/4096)	0x0100	ADC0GTH:ADC0GTL
	0x00FF	ADWINT not affected
	0x0000	
REF x (-1/4096)	0xFFFF	ADC0LTH:ADC0LTL
	0xFFFE	ADWINT=1
-REF	0xF800	

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 0,  
 ADC0LTH:ADC0LTL = 0xFFFF,  
 ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF or > 0x0100. (Two's Complement

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Figure 5.15: ADC Window Interrupt Examples, Left Justified Data

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0xFFFF0	ADWINT not affected
	0x2010	
REF x (512/4096)	0x2000	ADWINT=1
	0x1FFF0	
	0x1010	ADWINT=1
REF x (256/4096)	0x1000	
	0x0FF0	ADWINT not affected
0	0x0000	

Input Voltage (AD0 - AGND)	ADC Data Word	
REF x (4095/4096)	0xFFFF0	ADWINT=1
	0x2010	
REF x (512/4096)	0x2000	ADWINT not affected
	0x1FFF0	
	0x1010	ADWINT=1
REF x (256/4096)	0x1000	
	0x0FF0	ADWINT=1
0	0x0000	

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x2000,  
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0x1000.

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x1000,  
ADC0GTH:ADC0GTL = 0x2000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 or > 0x2000.

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x7FFF0	ADWINT not affected
	0x1010	
REF x (256/4096)	0x1000	ADWINT=1
	0x0FF0	
	0x0000	ADWINT=1
REF x (-1/4096)	0xFFFF0	
	0xFFE0	ADWINT not affected
-REF	0x8000	

Input Voltage (AD0 - AD1)	ADC Data Word	
REF x (4095/4096)	0x7FFF0	ADWINT=1
	0x1010	
REF x (256/4096)	0x1000	ADWINT not affected
	0x0FF0	
	0x0000	ADWINT=1
REF x (-1/4096)	0xFFFF0	
	0xFFE0	ADWINT=1
-REF	0x8000	

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0x1000,  
ADC0GTH:ADC0GTL = 0xFFFF0.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 and > 0xFFFF0. (Two's Complement math.)

Given:

AMX0SL = 0x00, AMX0CF = 0x01, ADLJST = 1,  
ADC0LTH:ADC0LTL = 0xFFFF0,  
ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0xFFFF0 or > 0x1000. (Two's Complement math.)

are given in Table 0.1.

Figure 6.1. DAC Functional Block Diagram

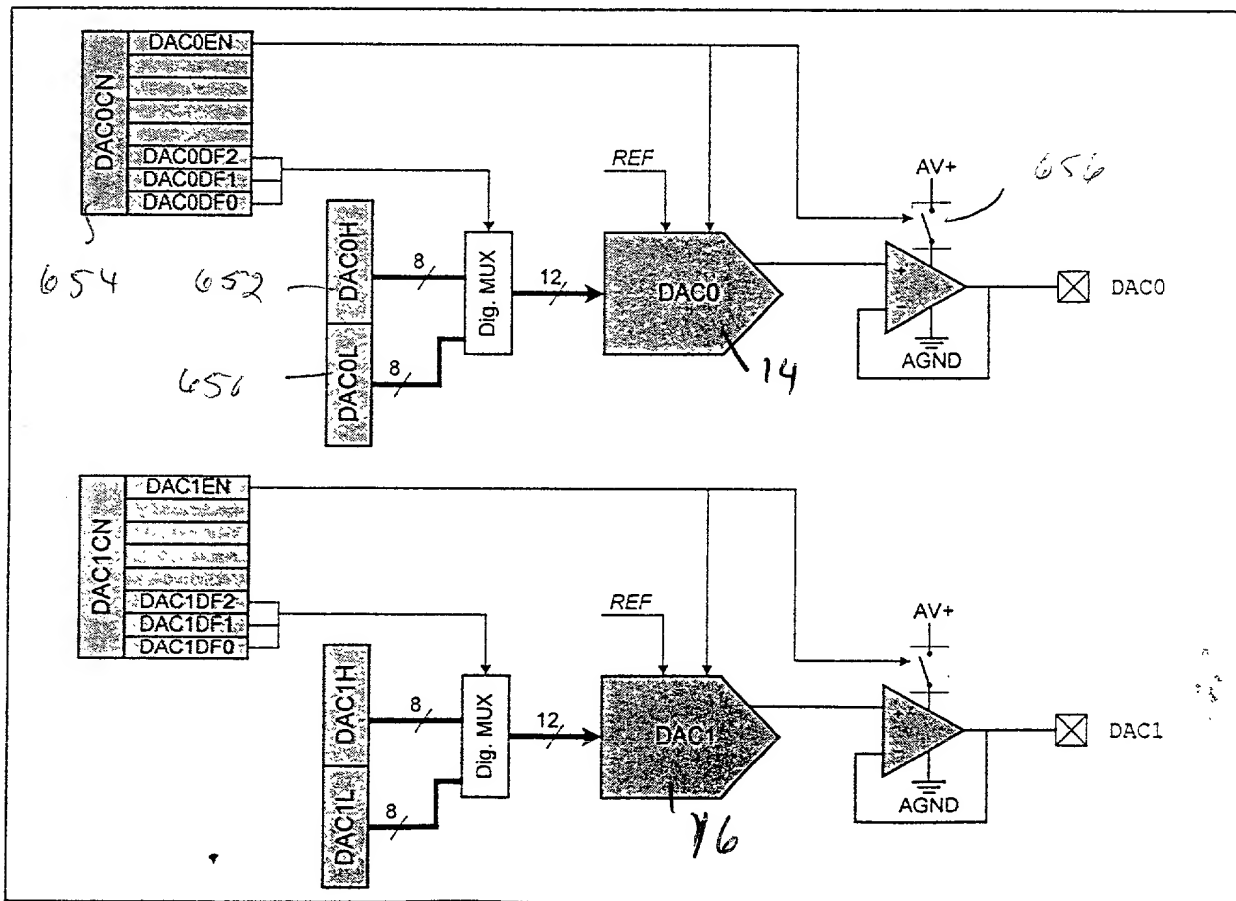
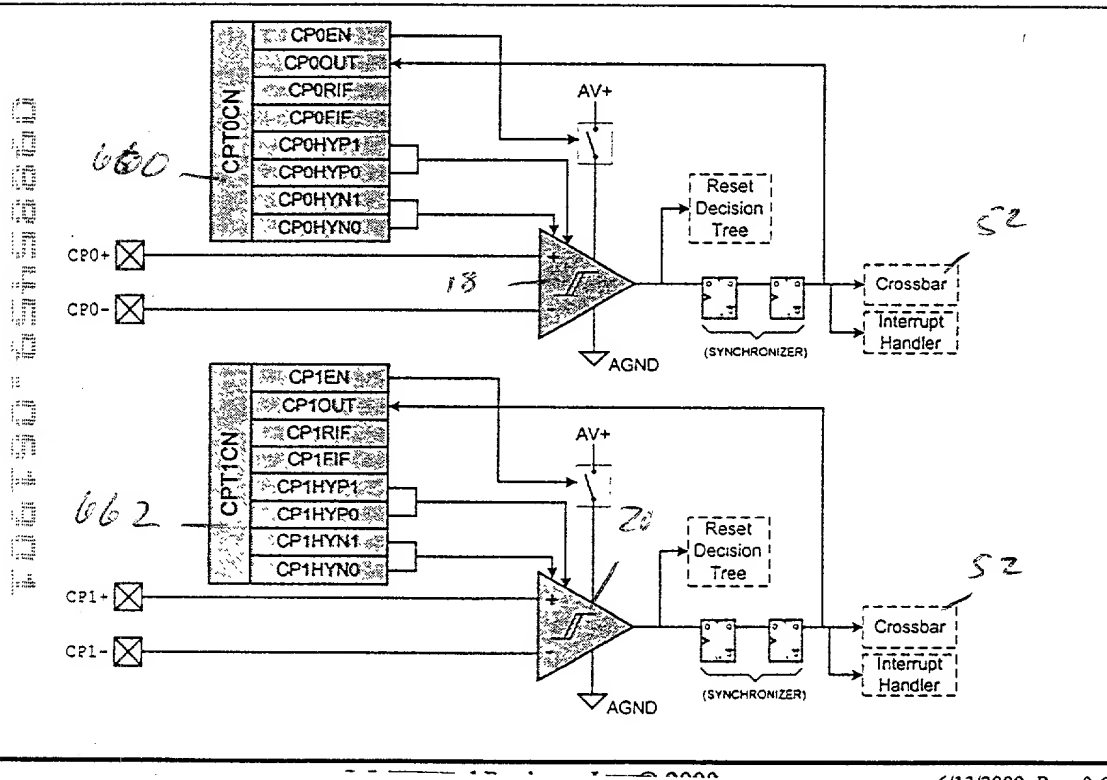


Figure 7.1. Comparator Functional Block Diagram



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Figure 7.2. Comparator Hysteresis Plot

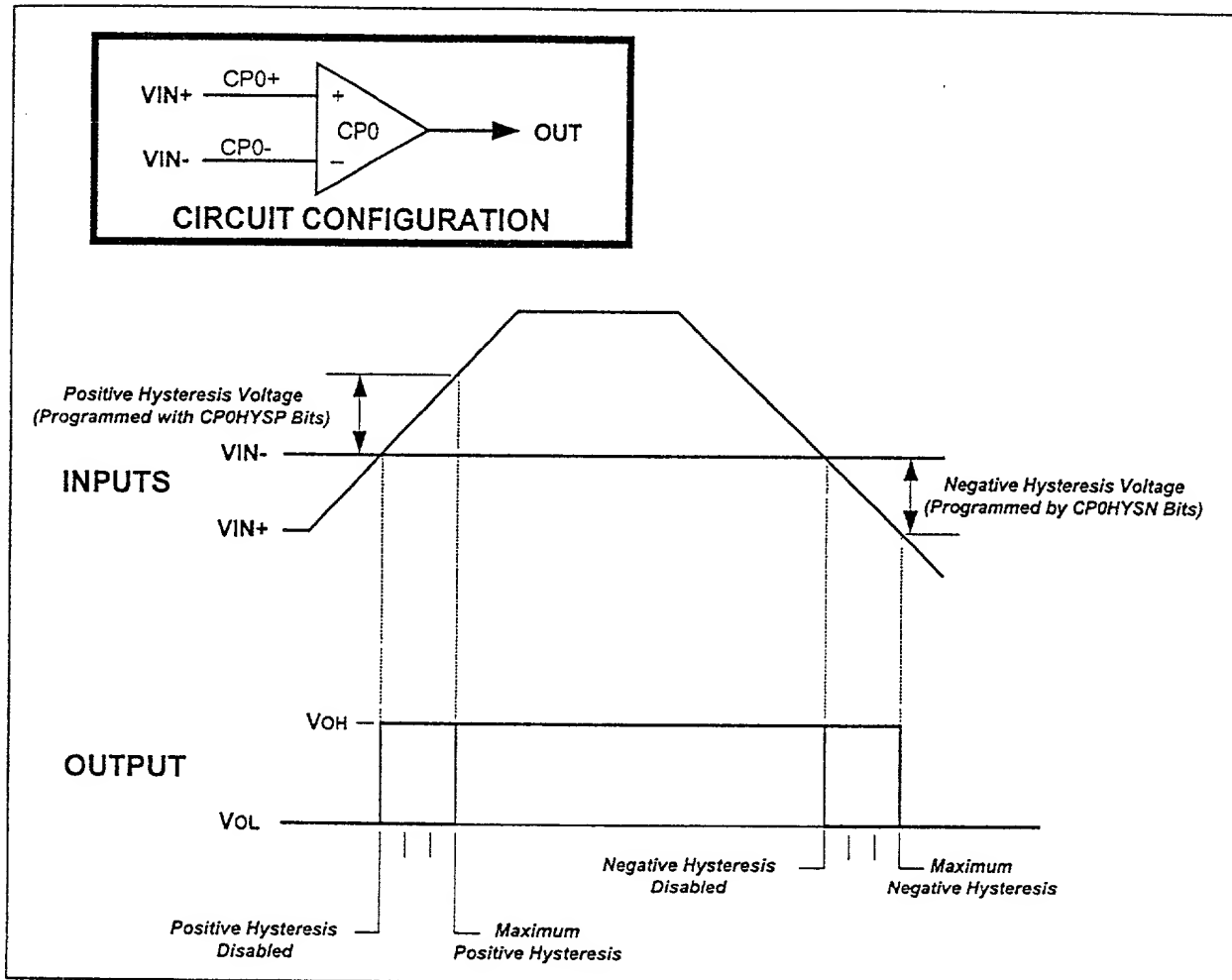


Figure 8.1. Voltage Reference Functional Block Diagram

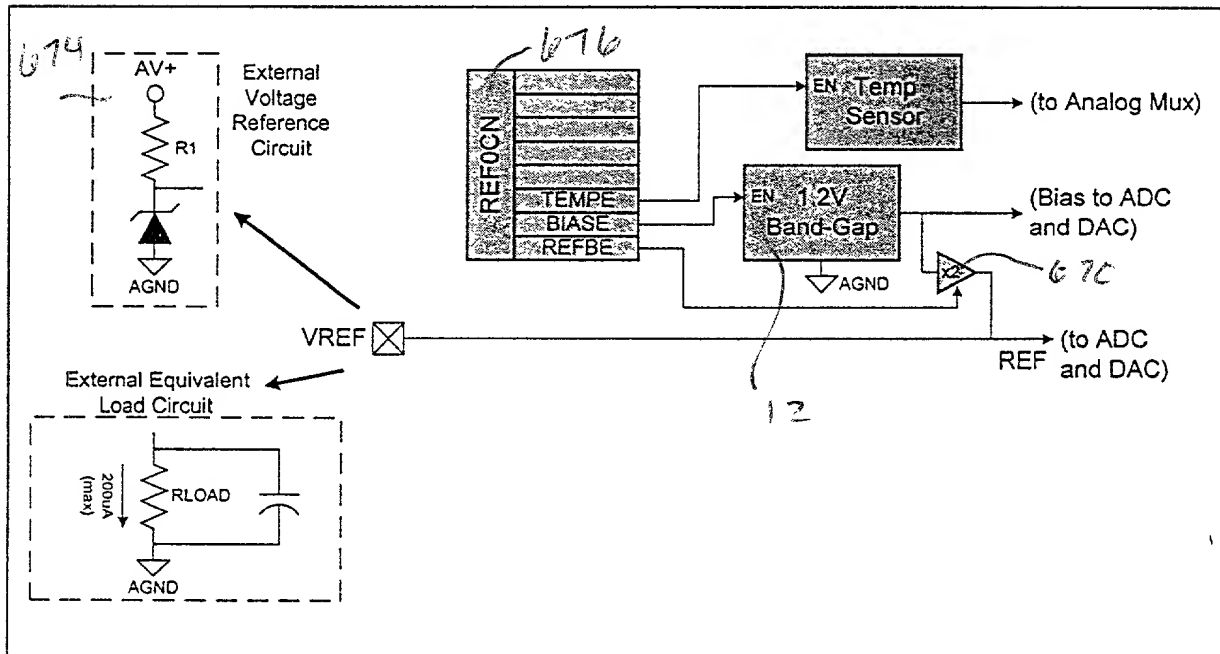
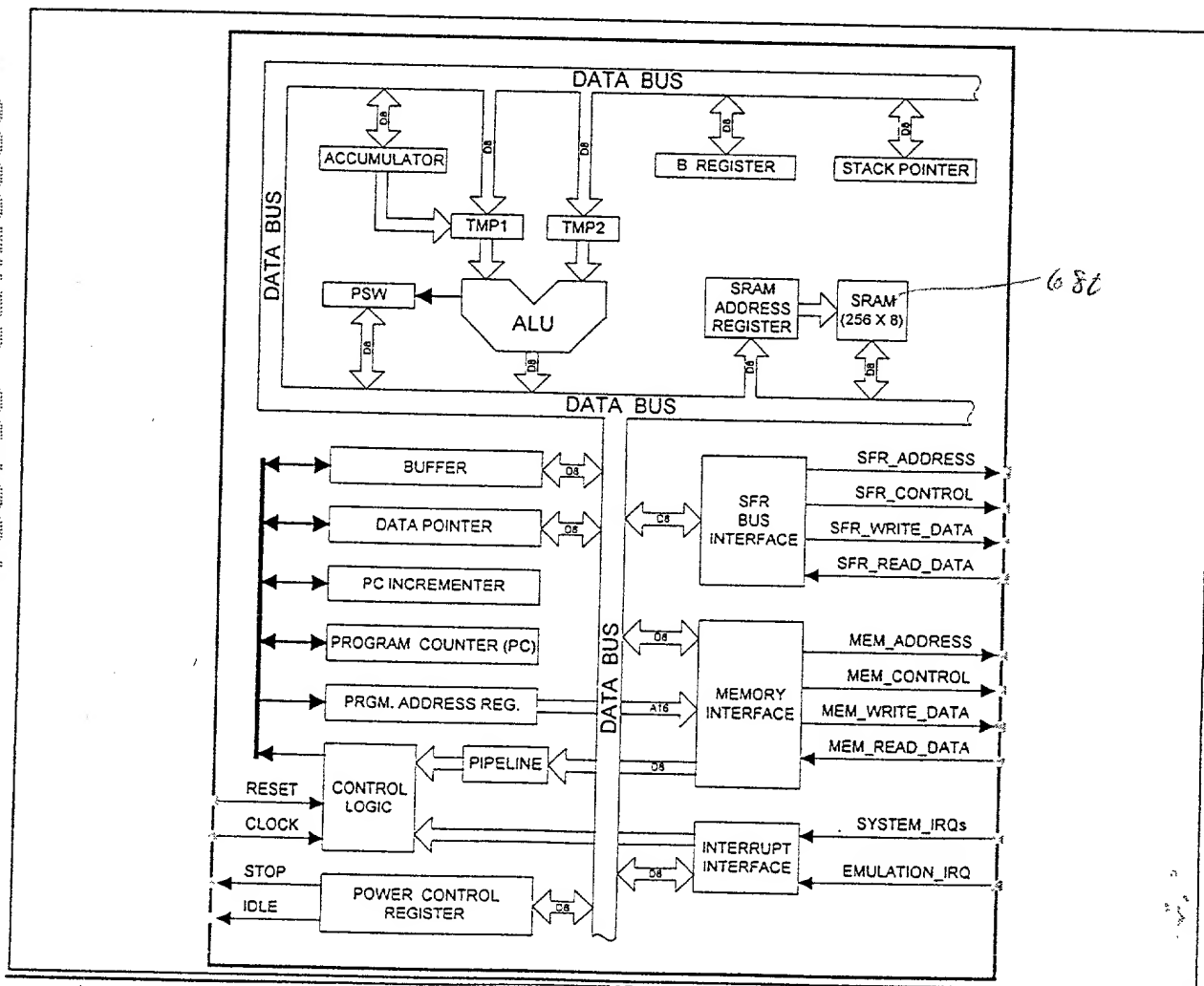


Figure 21. CIP-51 Block Diagram



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25 36  
Figure 22. Memory Map

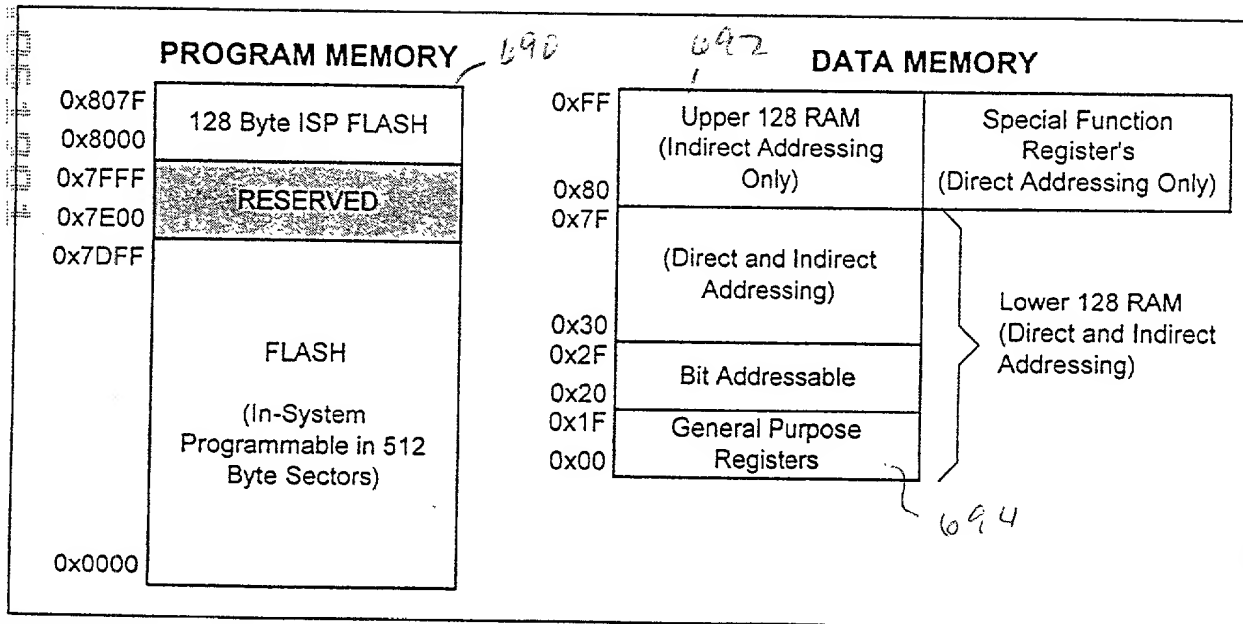
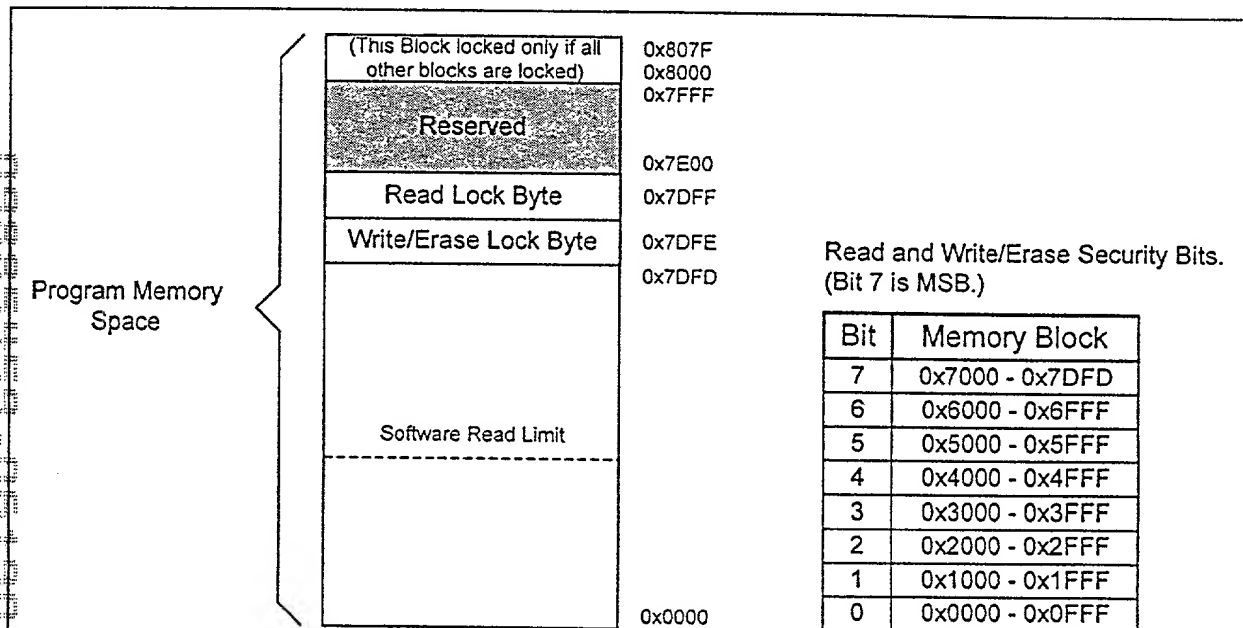


FIGURE 10.1

Figure 10.1. Flash Program Memory Security Bytes



#### FLASH Read Lock Byte

Bits7-0: Each bit locks a corresponding block of memory. (Bit 7 is MSB.)

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

#### FLASH Write/Erase Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

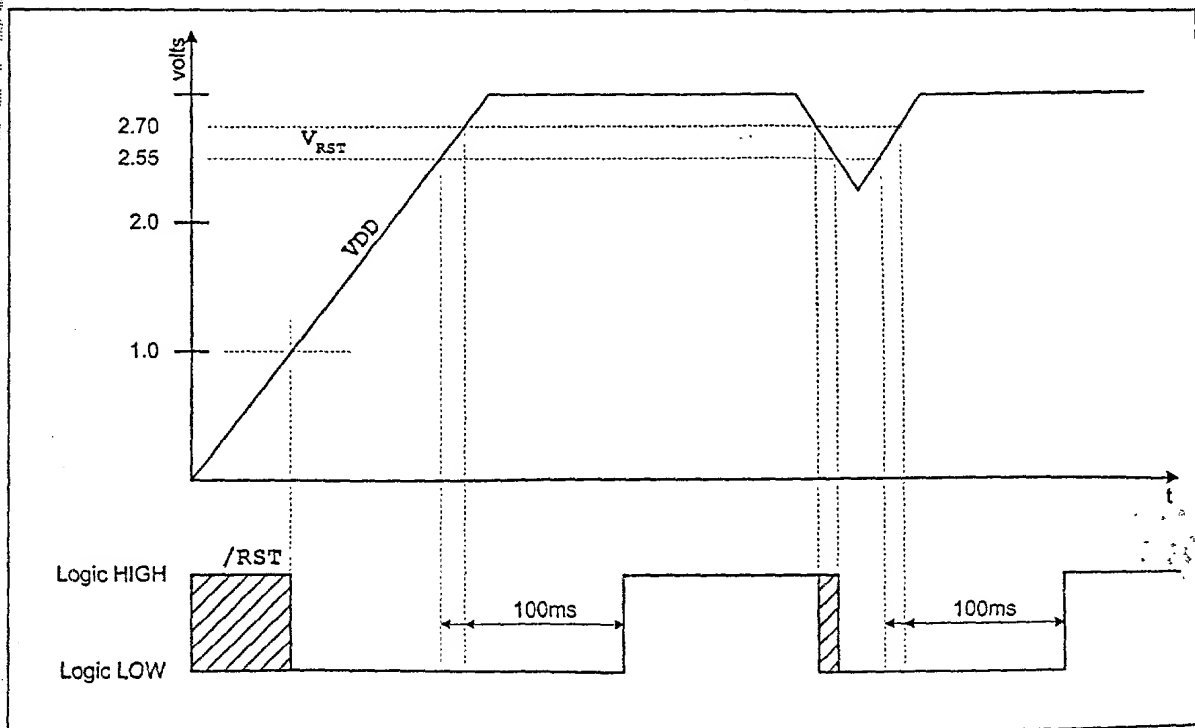
1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

#### FLASH Access Limit Register (FLACL)

The content of this register is used as the high byte of the 16-bit software read limit address. The 16-bit read limit address value is calculated as 0xNN00 where NN is replaced by content of this register on reset. Software running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase, locations below this address. Any attempts to read locations below this limit will return the value 0x00.

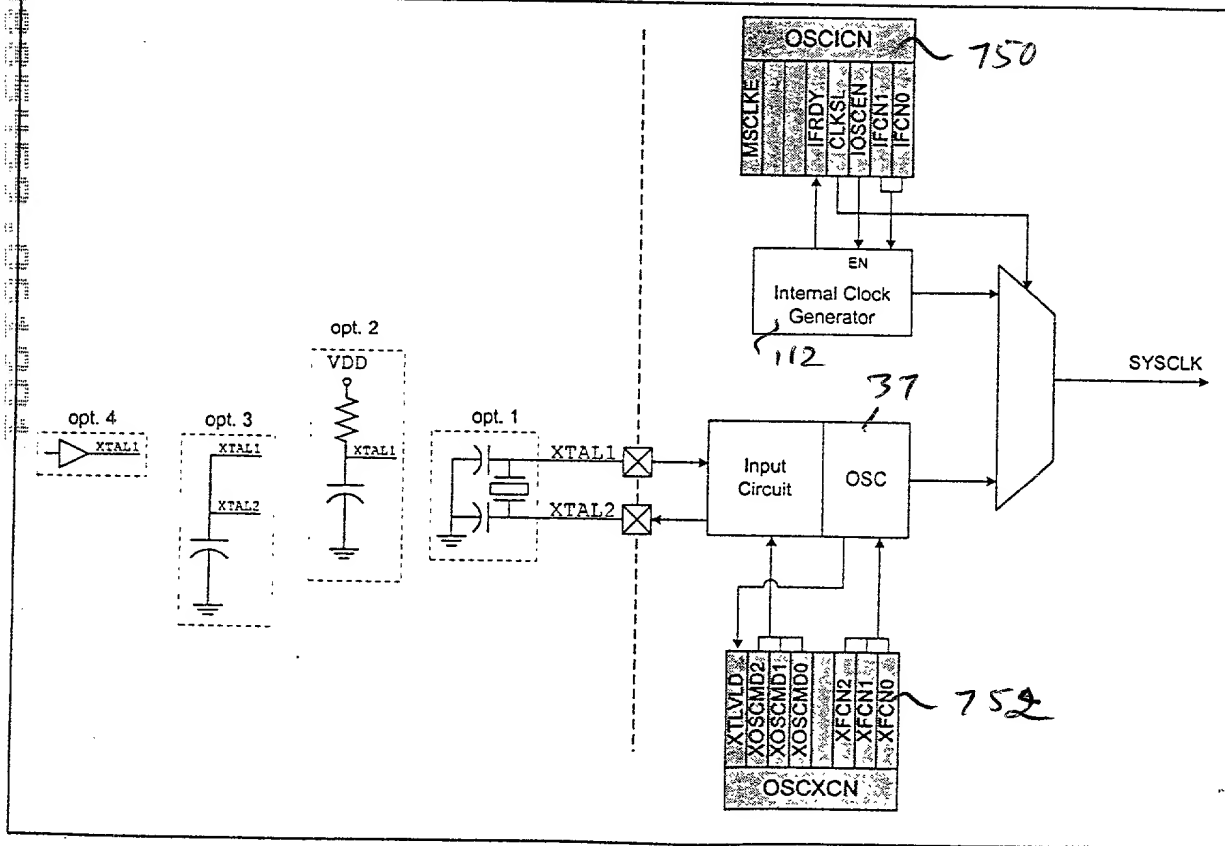
22  
86

Figure 11.2. VDD Monitor Timing Diagram



23  
21

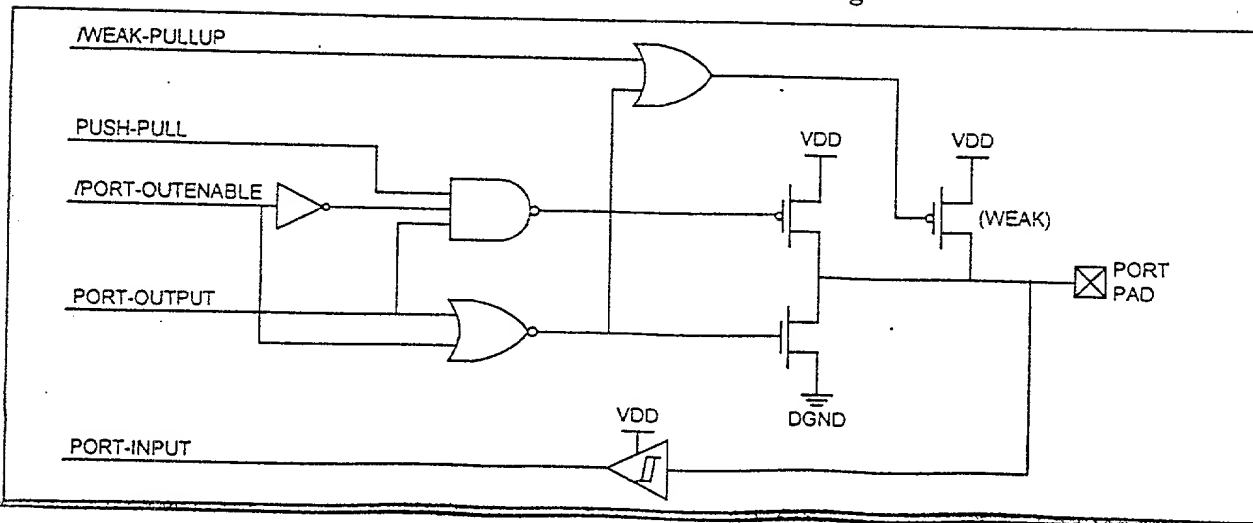
Figure 12.1. Oscillator Diagram



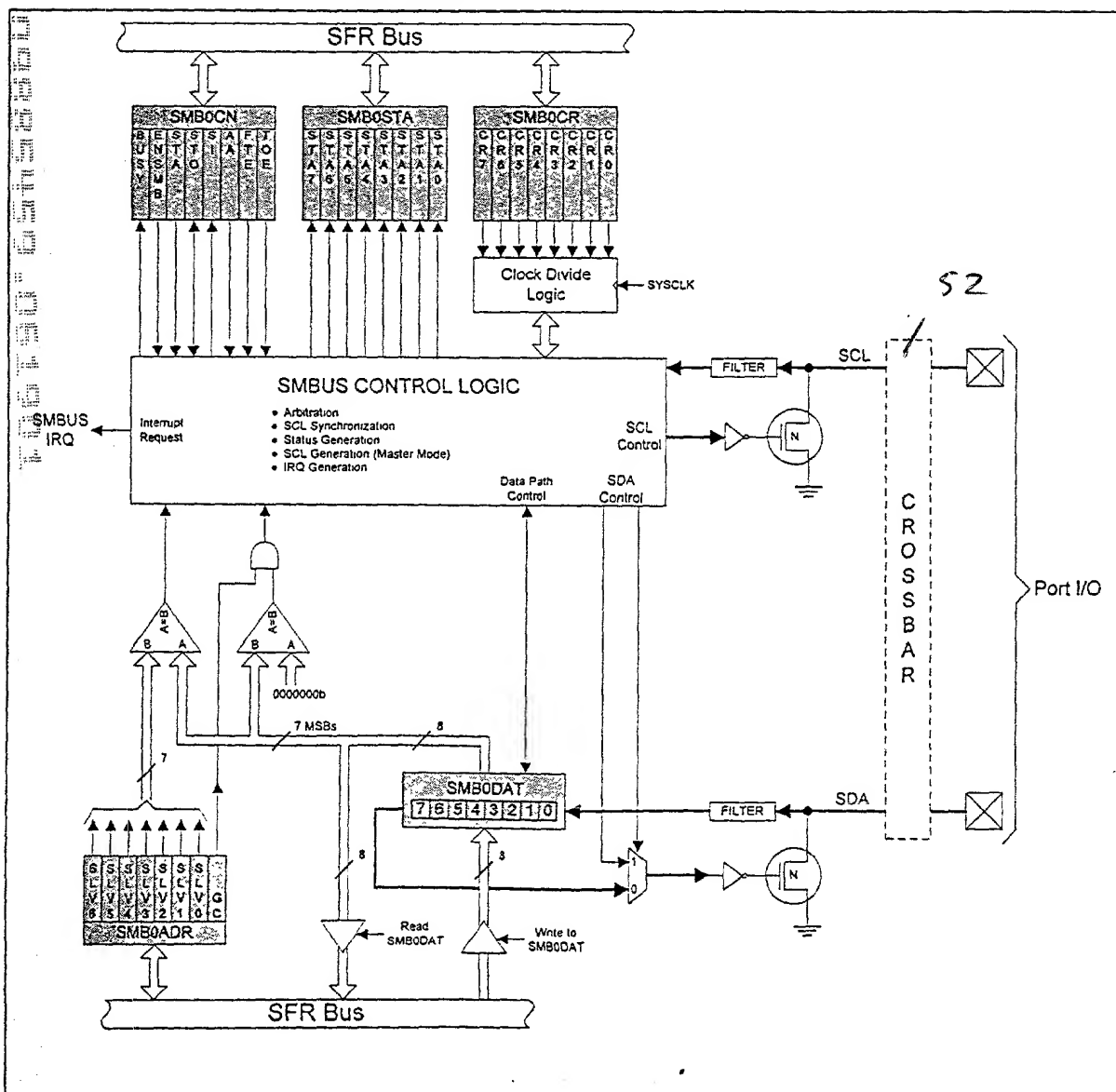
PORTPAD=6458660

3928

Figure 13.2. Port I/O Cell Block Diagram

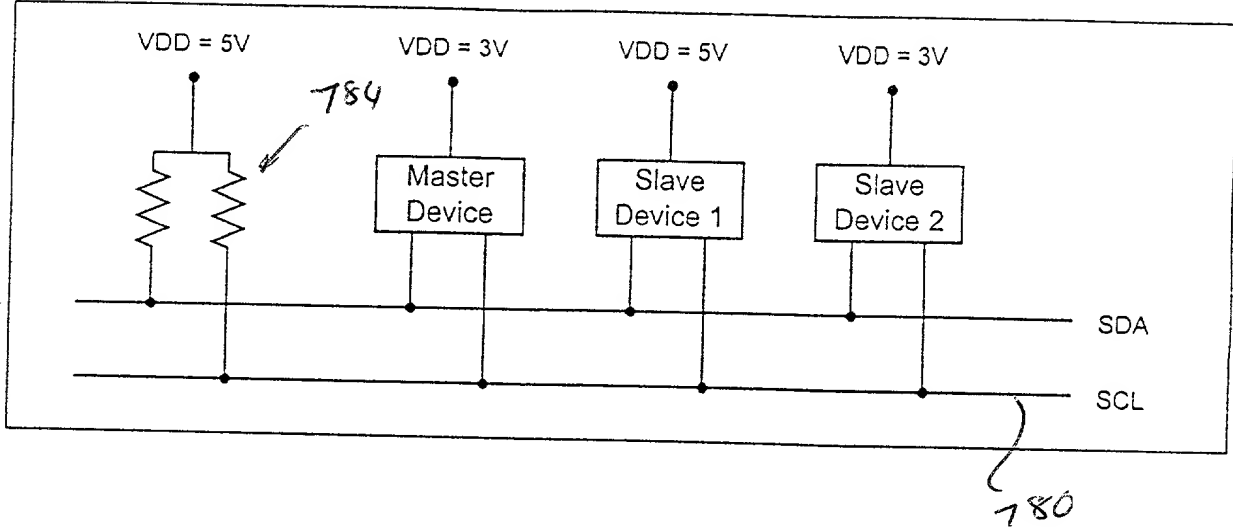


**Figure 14.1. SMBus Block Diagram**



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Figure 14.2. Typical SMBus Configuration

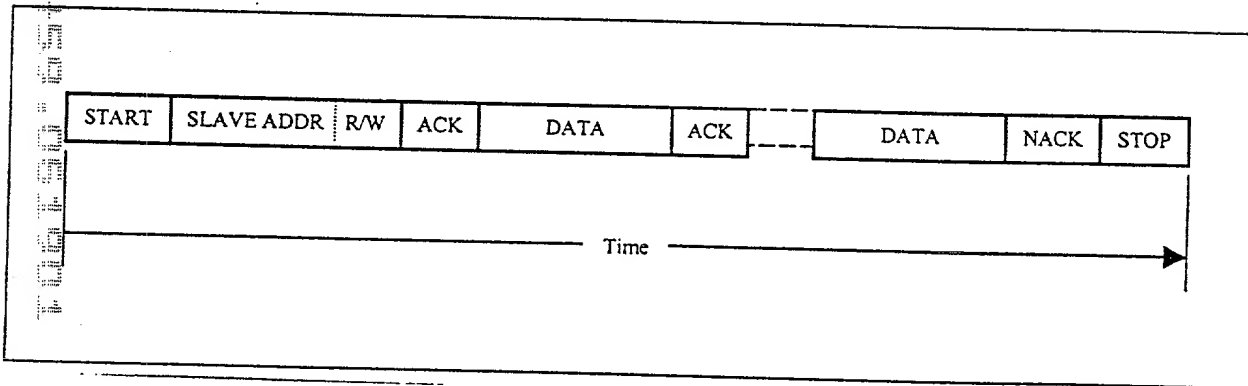


100750 645000

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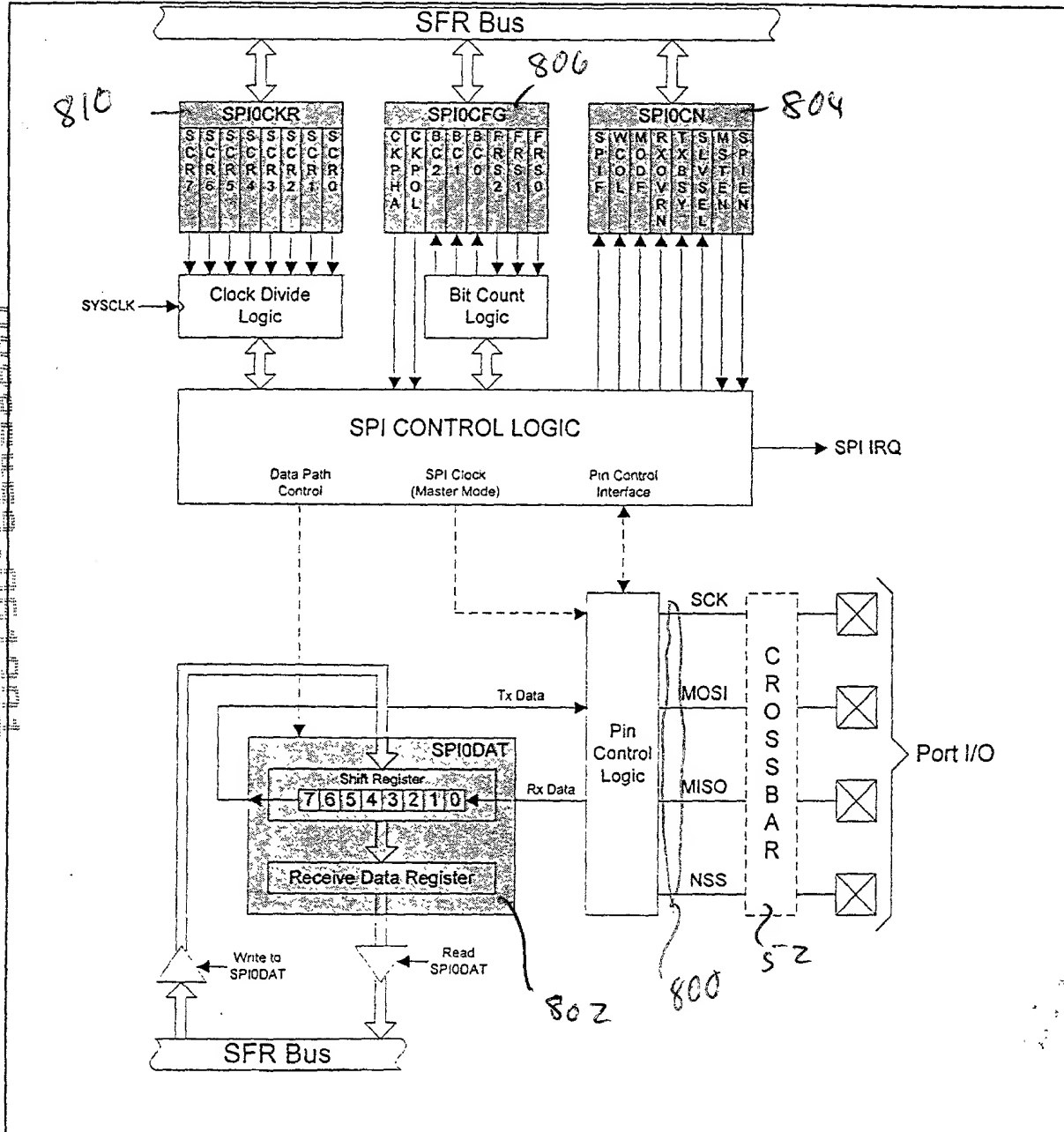
B2  
~~42~~

Figure 14.3. SMBus Transaction



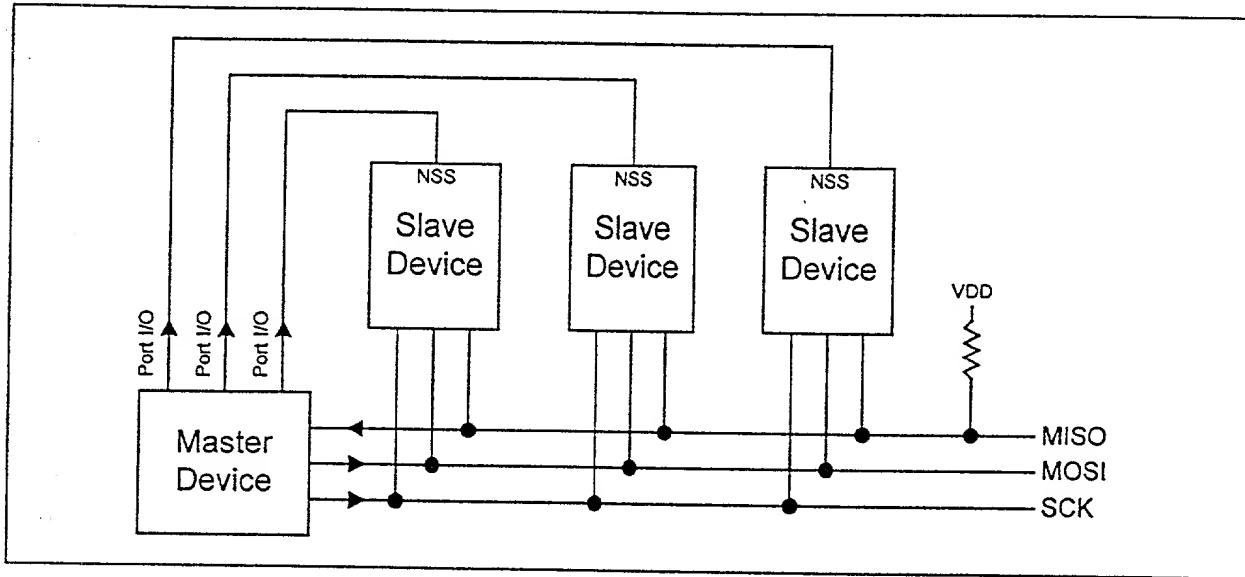
CCDA 25,768  
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28  
29  
Figure 15.1. SPI Block Diagram



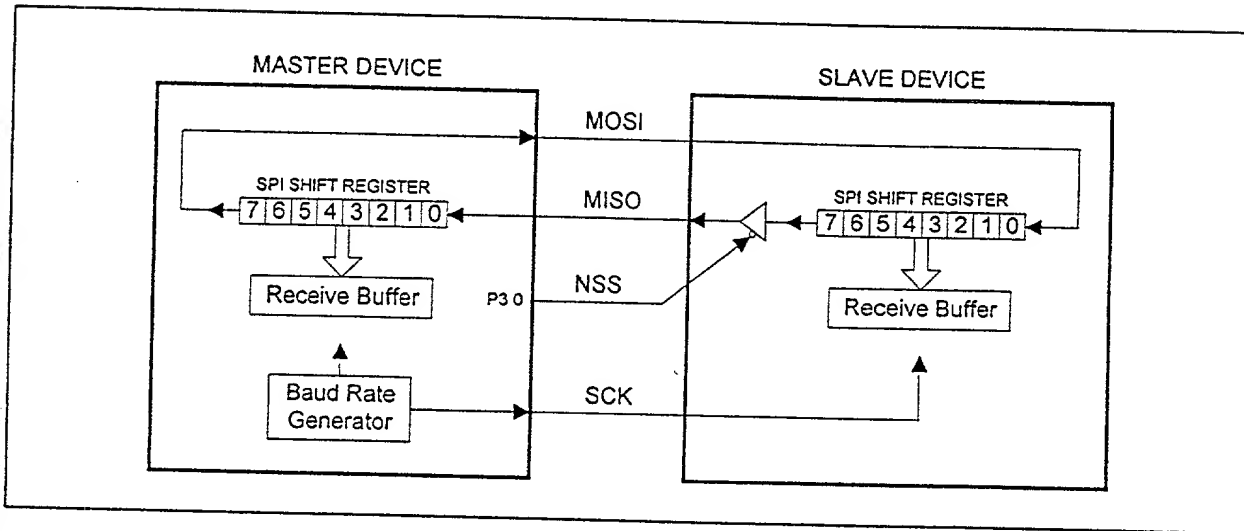
30 36 29

Figure 15.2. Typical SPI Interconnection



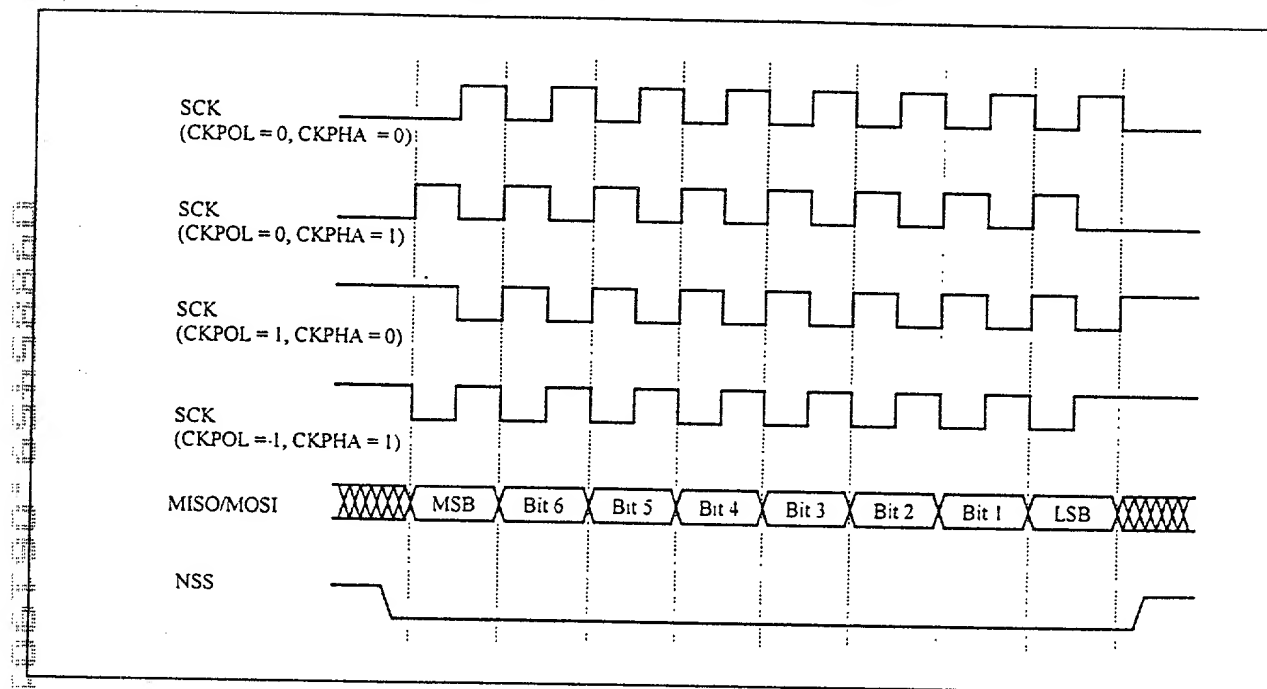
30

Figure 15.3. Full Duplex Operation



31  
~~32~~  
20

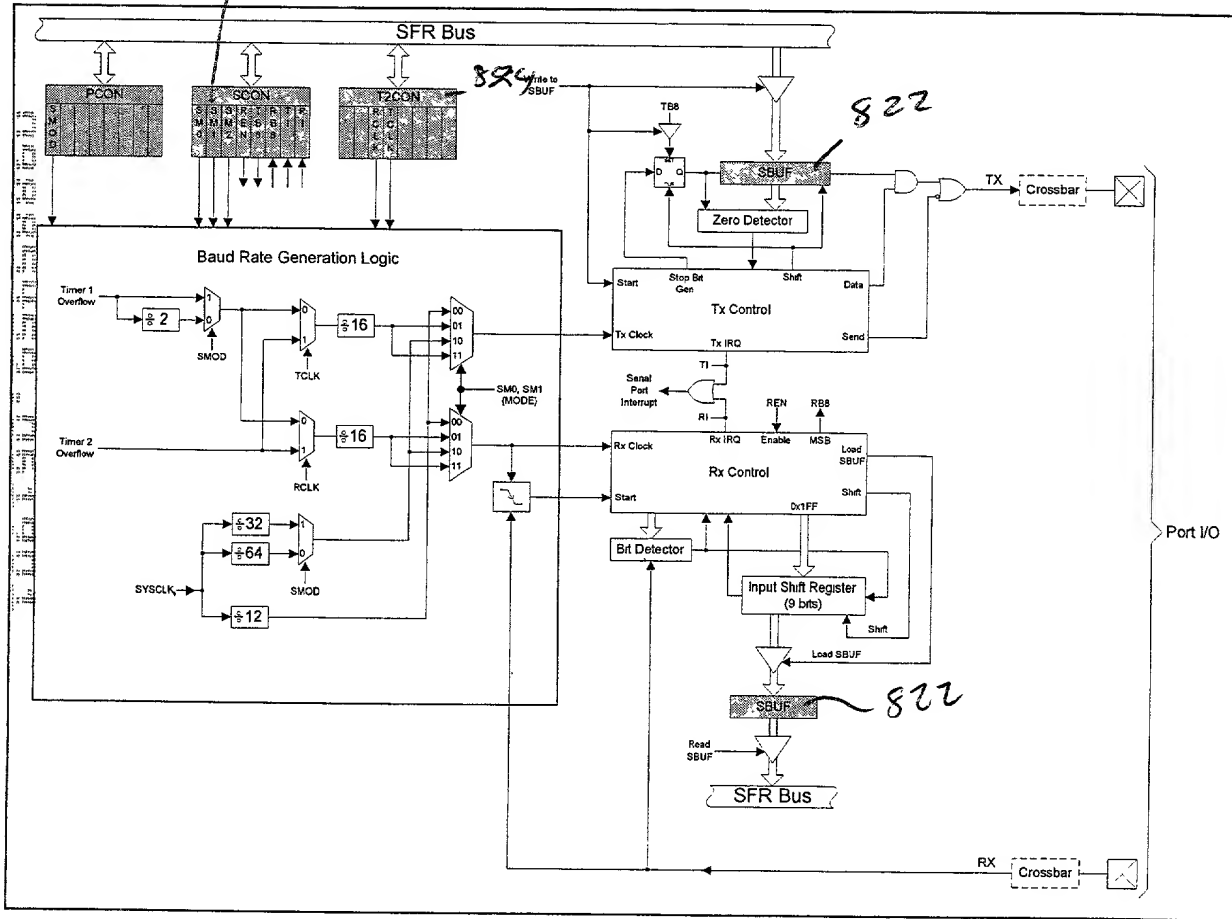
Figure 15.4. Data/Clock Timing Diagram



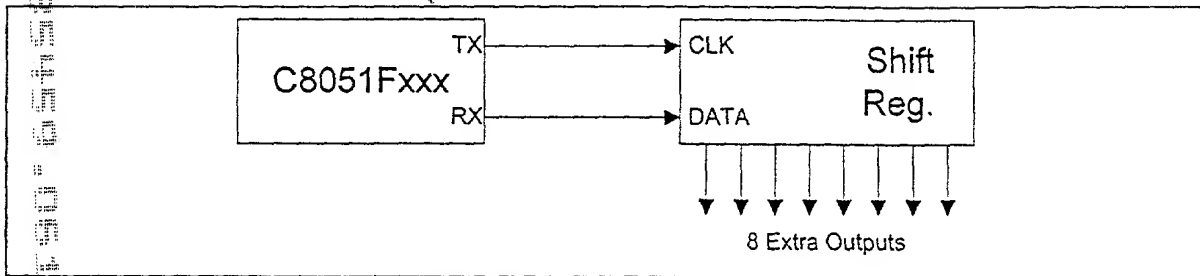
820

FIG 32

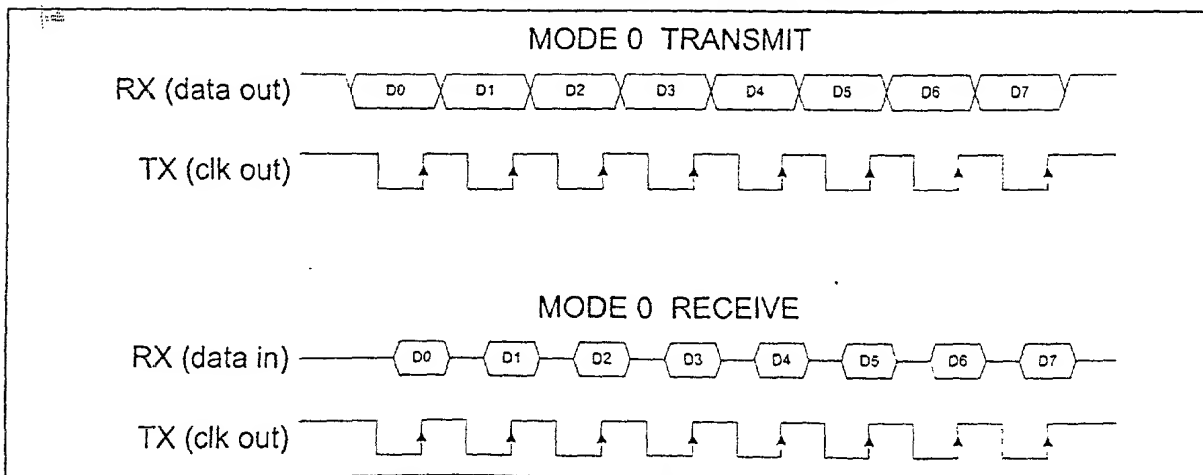
Figure 10.1. UAK1 Block Diagram



33  
34  
35  
Figure 16.2. UART Mode 0 Interconnect

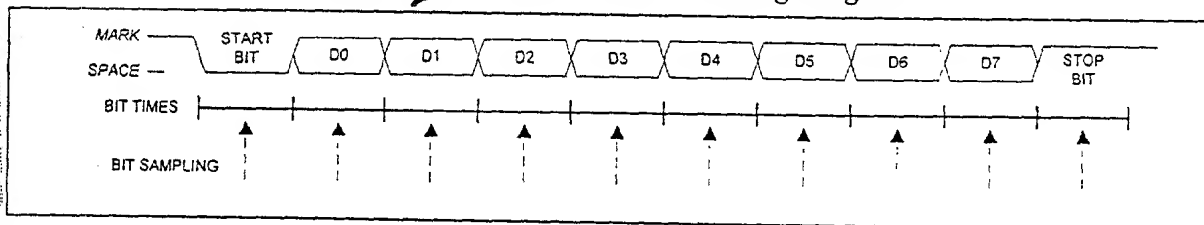


34  
35  
36  
Figure 16.3. UART Mode 0 Timing Diagram



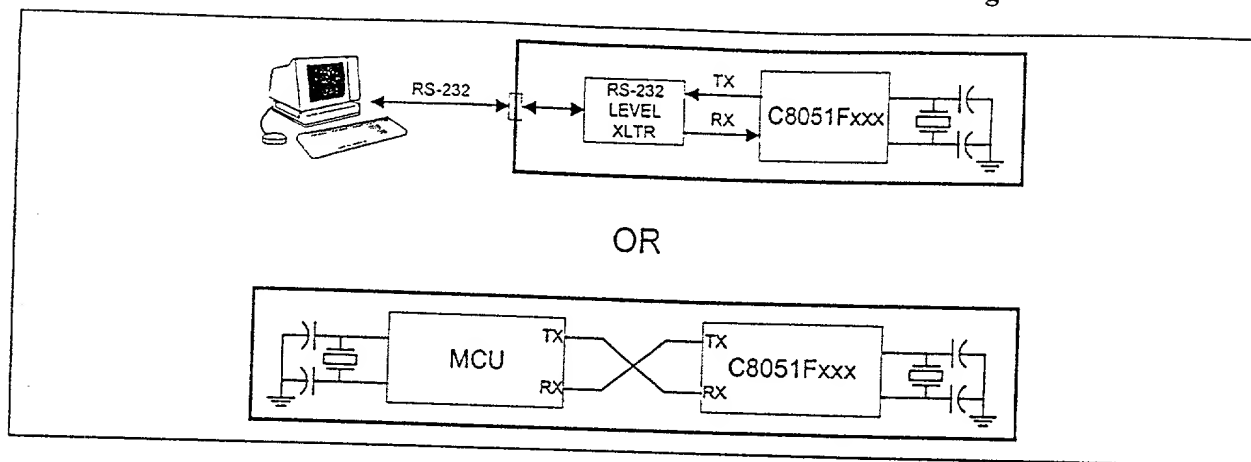
CCDA 25,768  
34/50

35 ~~33~~  
40  
Figure 16.4. UART Mode 1 Timing Diagram

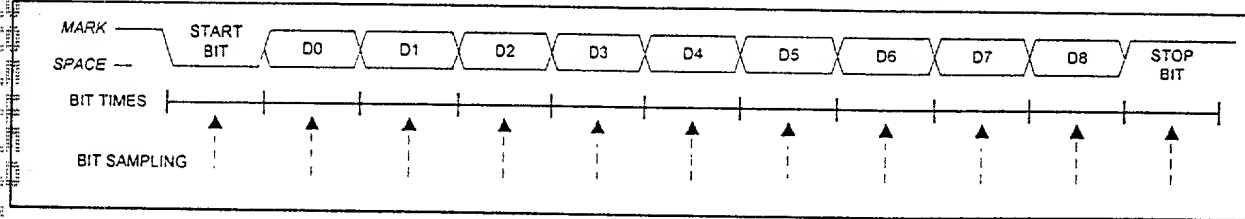


36  
41

Figure 16.5. UART Modes 1, 2, and 3 Interconnect Diagram



37  
42  
Figure 16.6. UART Modes 2 and 3 Timing Diagram



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38  
47

Figure 16.7. UART Multi-Processor Mode Interconnect Diagram

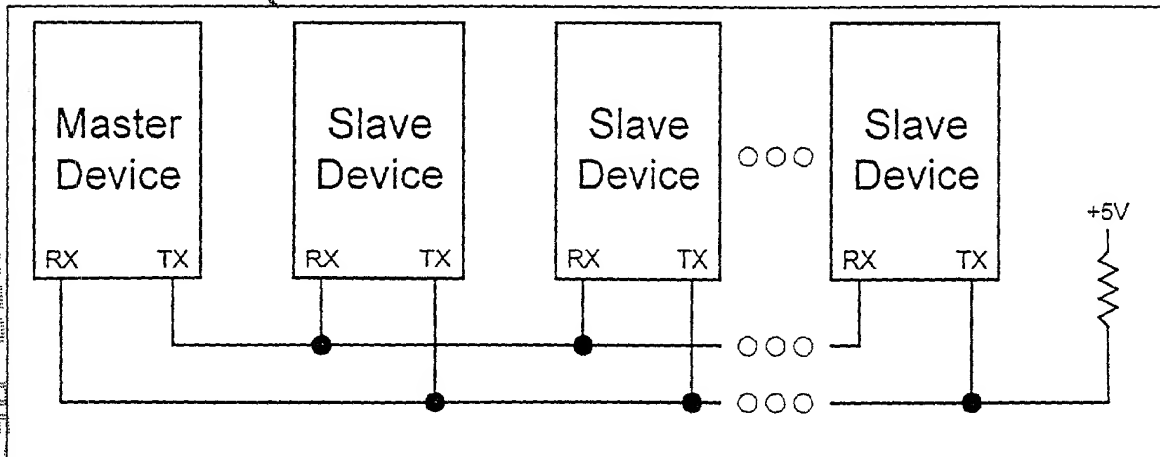
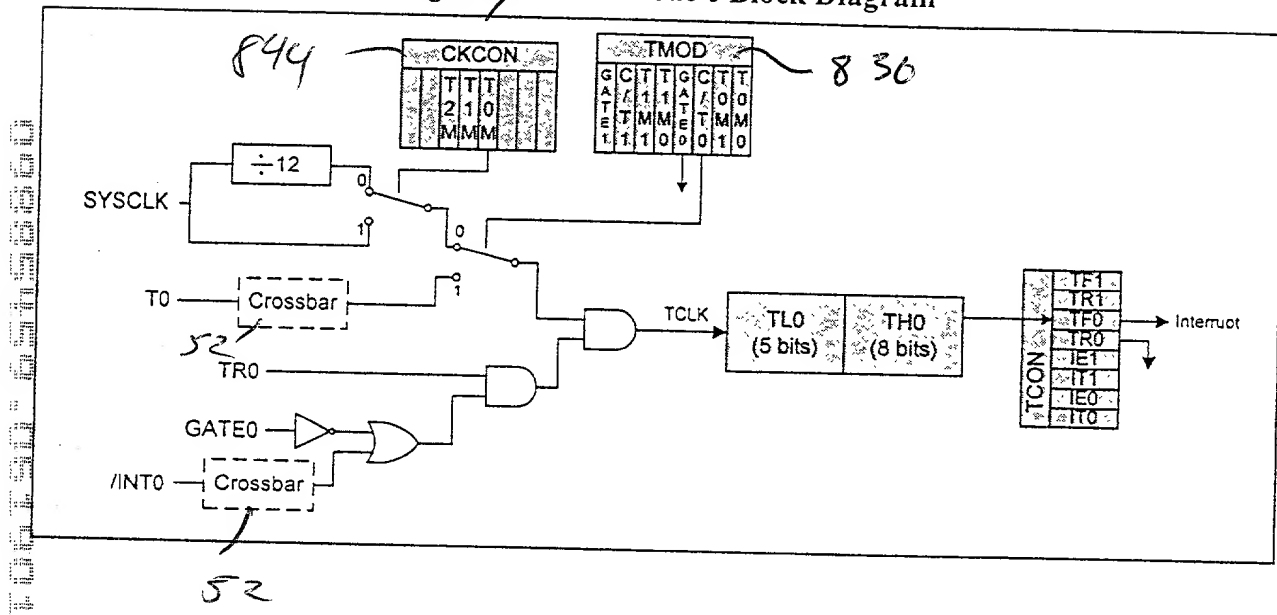


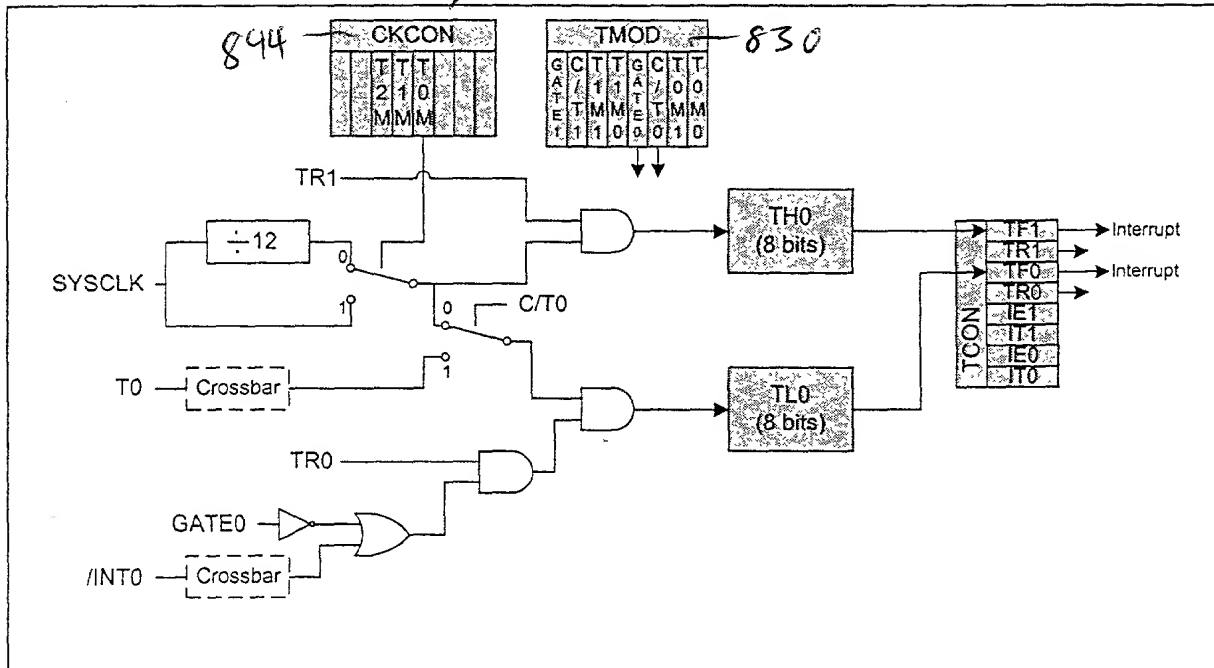
Figure 17.1. T0 Mode 0 Block Diagram



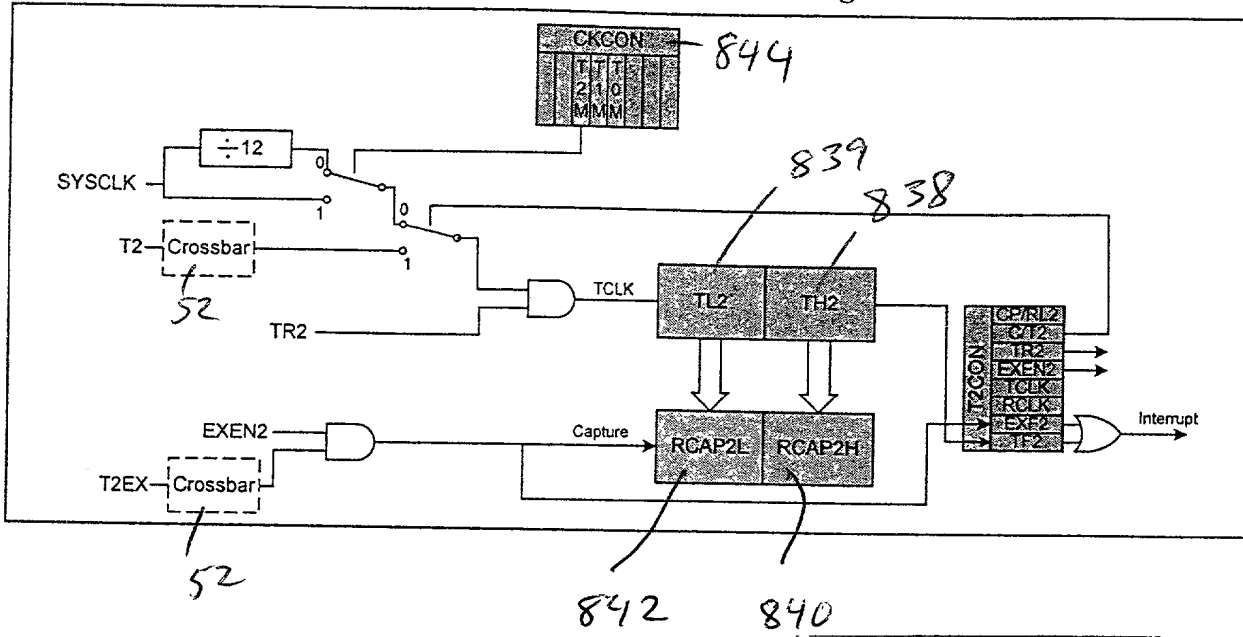


41  
~~40~~

Figure 17.3. T0 Mode 3 Block Diagram



42  
41  
Figure 17.11. T2 Mode 0 Block Diagram



43

46

Figure 17.12. T2 Mode 1 Block Diagram

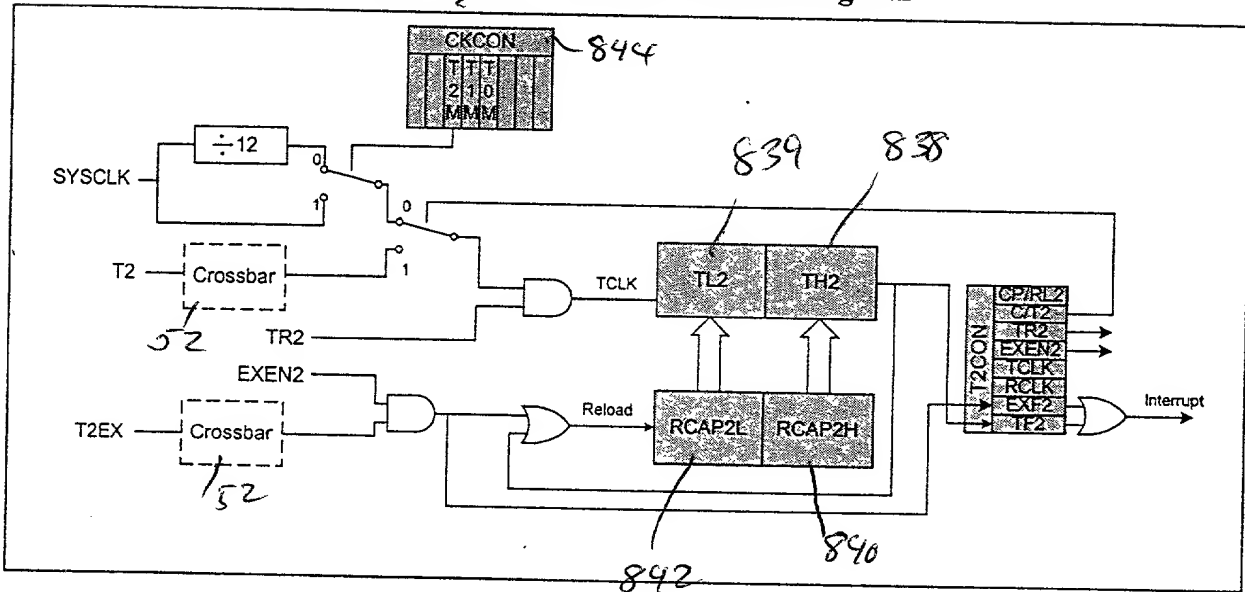
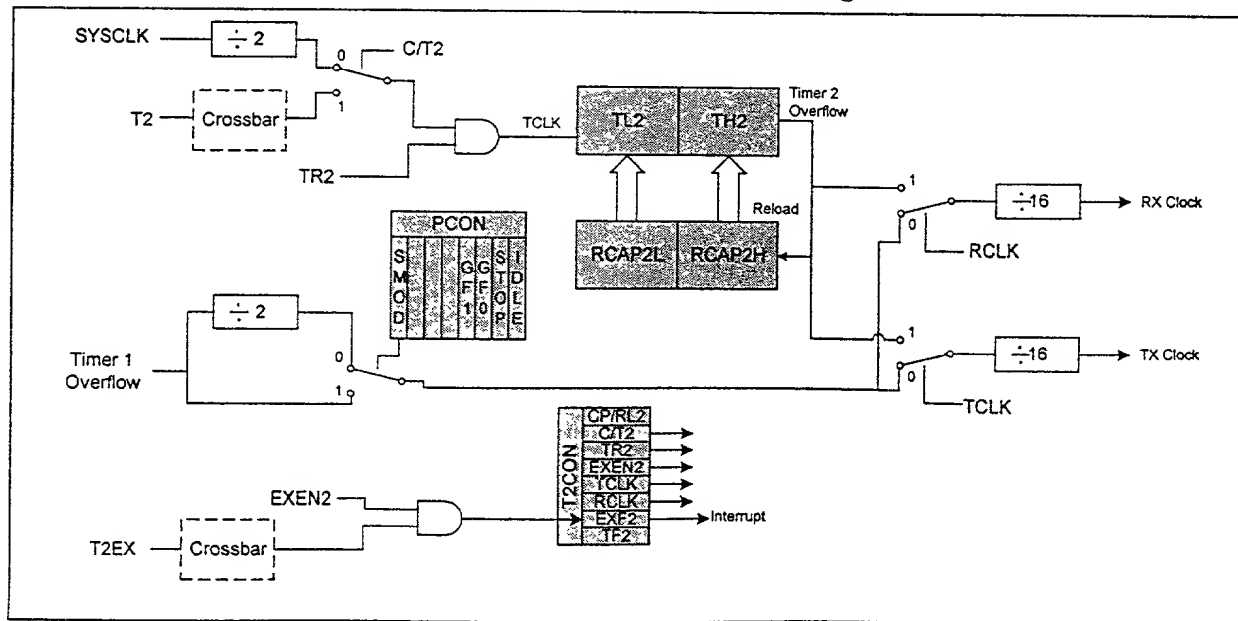


Figure 17.13. T2 Mode 2 Block Diagram



45  
Figure 17.19. Timer 3 Block Diagram

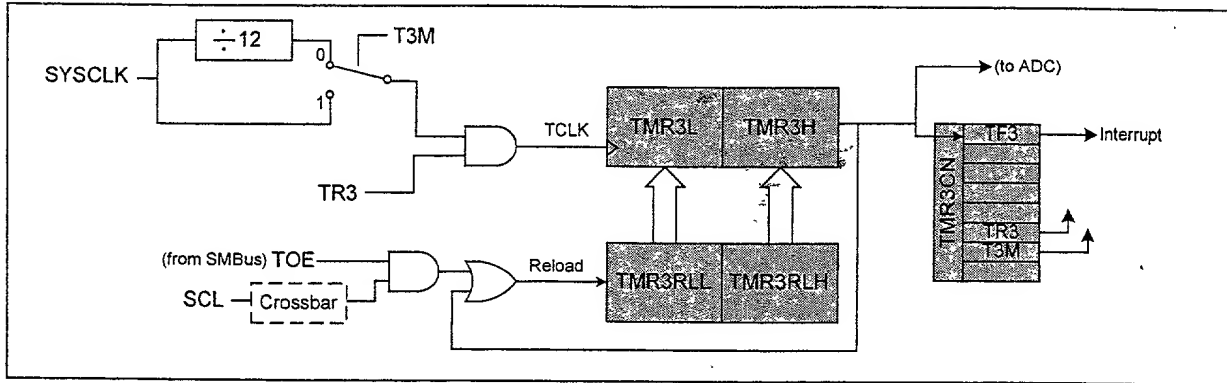
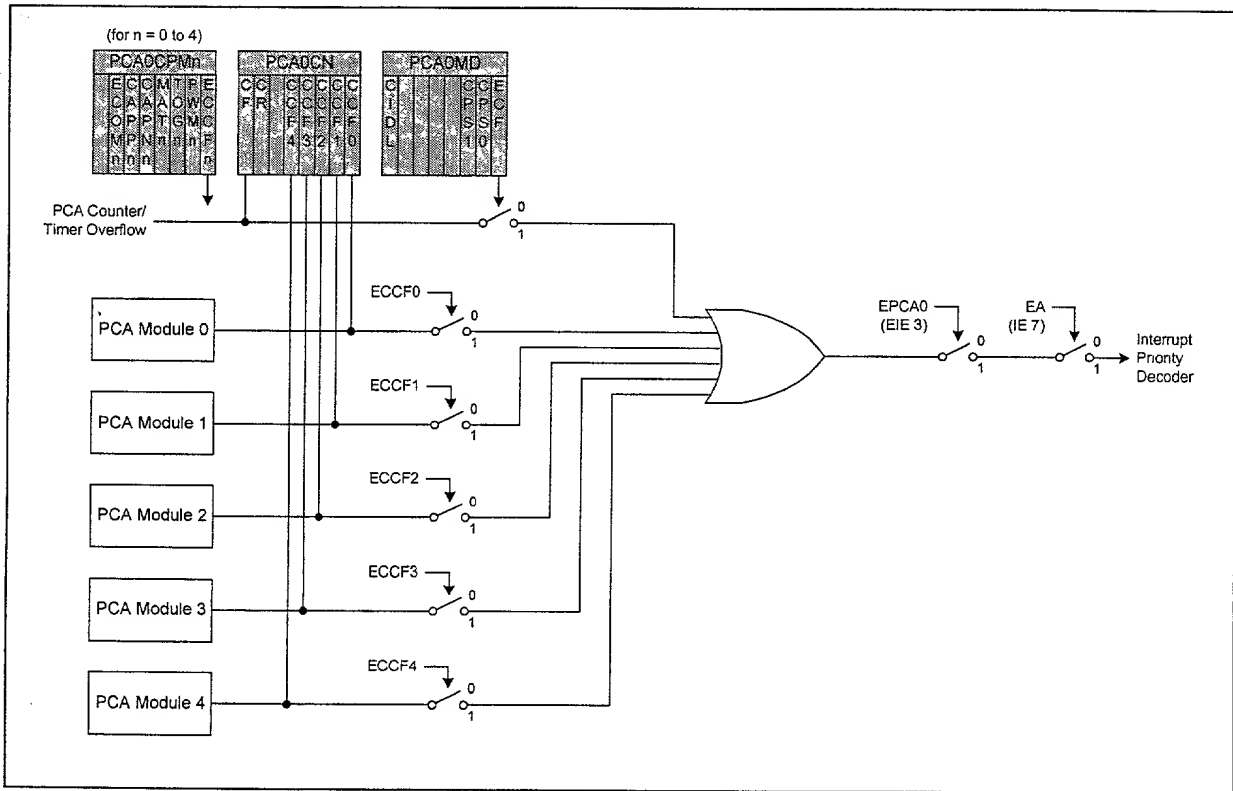
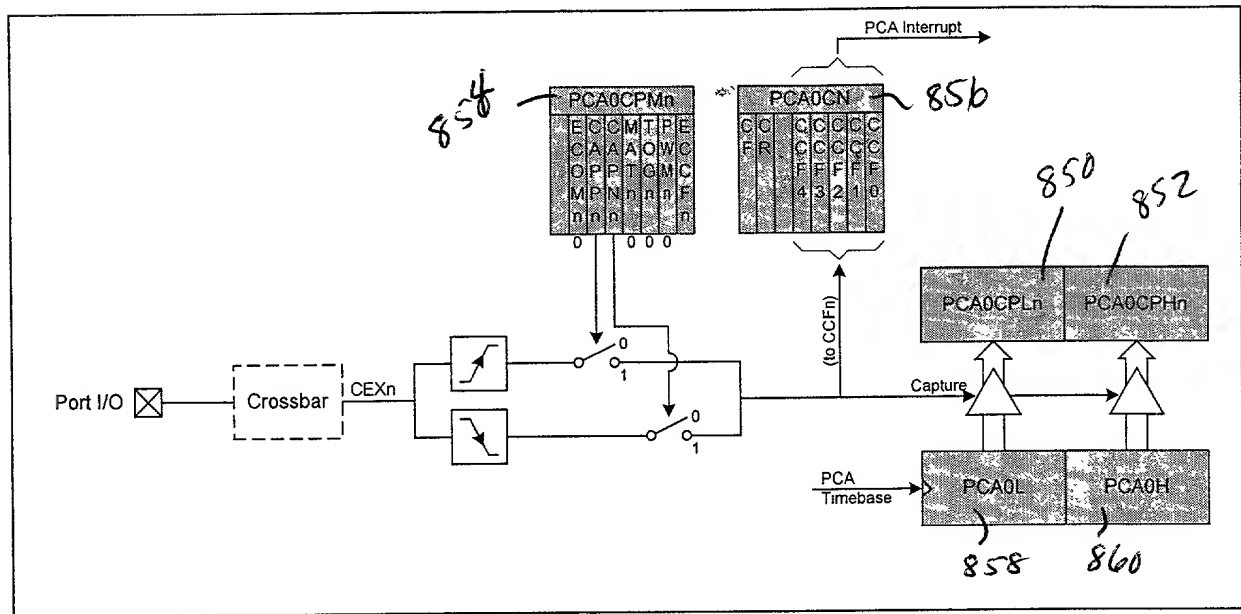


FIGURE 46



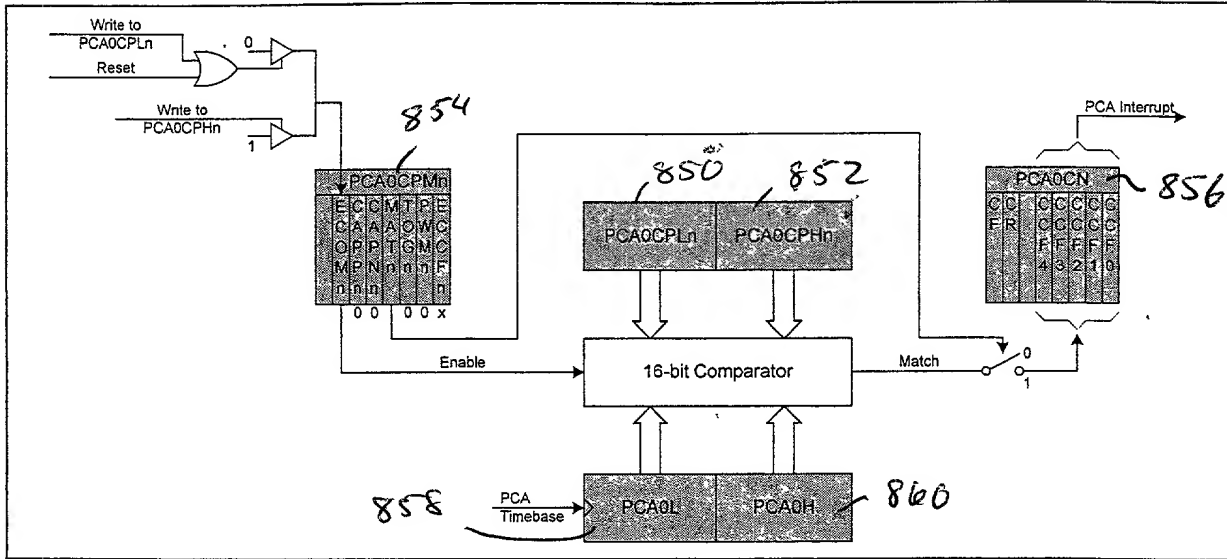
47

Figure 18.3. PCA Capture Mode Diagram

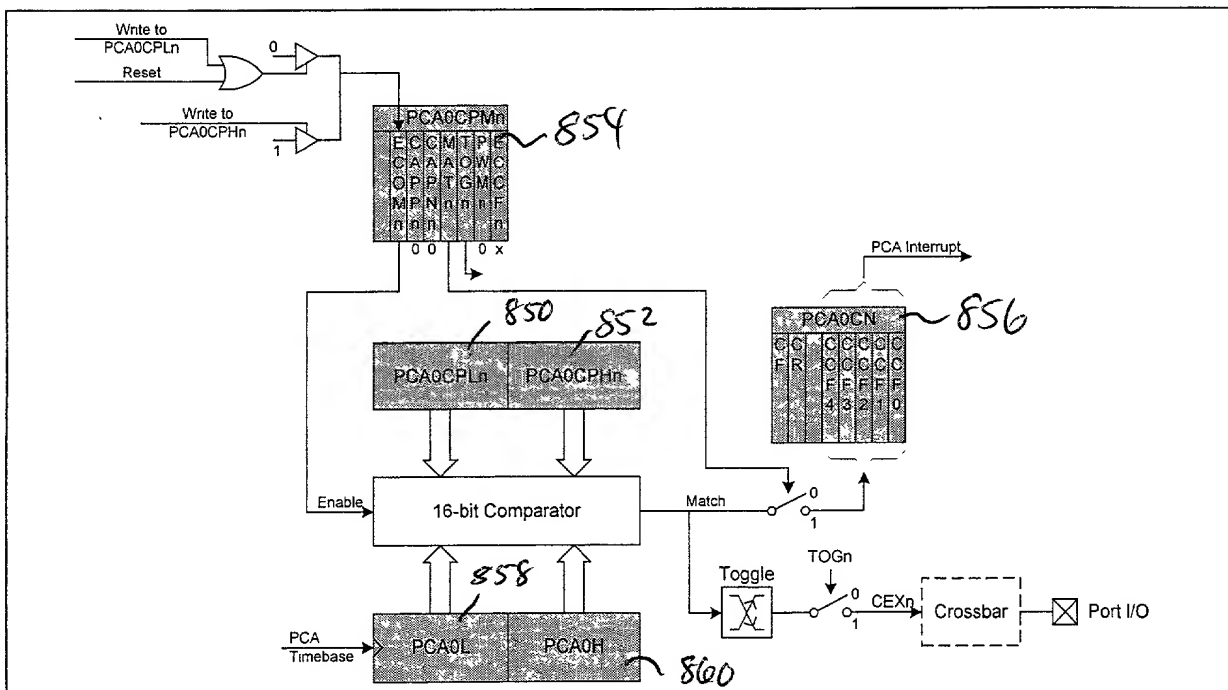


48

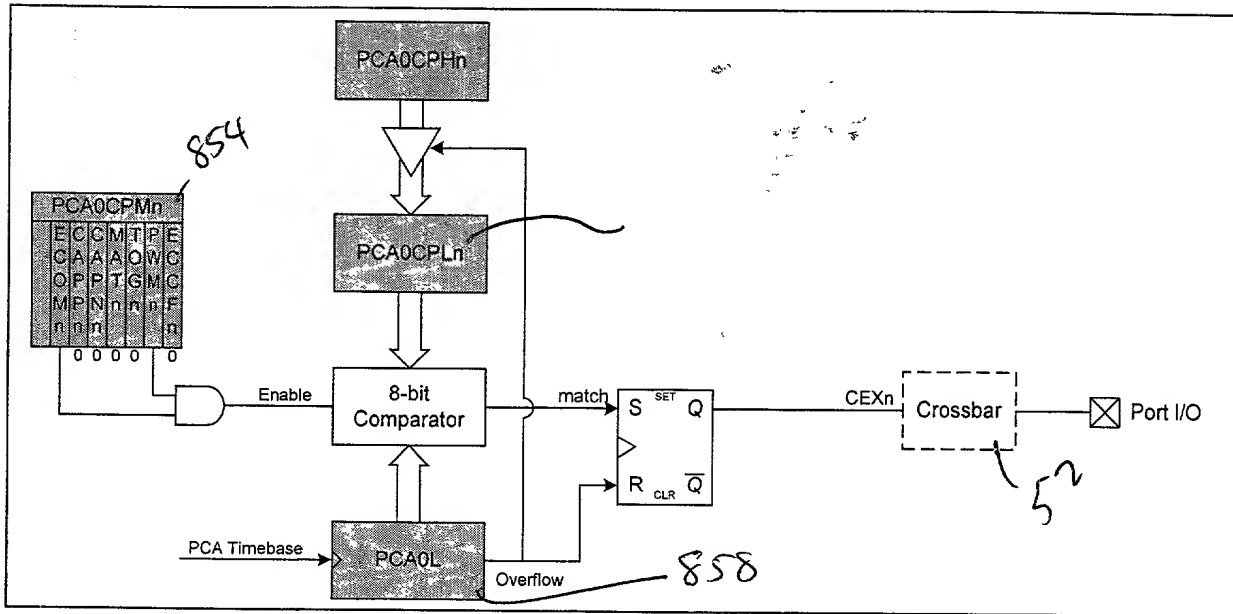
Figure 18.4. PCA Software Timer Mode Diagram



49  
50  
Figure 18.5. PCA High Speed Output Mode Diagram



50  
Figure 186. PCA PWM Mode Diagram



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Figure 18.7. PCA Counter/Timer Block Diagram

